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1 INTRODUCTION

1.1 Scope

With the growth of intelligent transportation systems (ITS), transportation management increasingly relies on electronically controlled devices deployed in the field and the controllers that coordinate and relay data from those devices. The ATC Controller Standard describes a family of advanced ruggedized field communications and process controllers that are configurable for a variety of traffic management applications. Typically, they provide communication, control, and data gathering from and to

- Central control computers when appropriate
- Other ATC Controller controllers when appropriately configured
- Control units for devices deployed in the field, typically in the vicinity of and linked to the controller.

Essentially an ATC Controller is a special function computer that must be able to operate remotely in a largely unattended mode in the harsh environment of field deployments throughout the United States.

The goal of this standard is to provide a next generation open architecture design for the next generation of transportation controller applications. These controllers are modular in design and intended to be compatible with or inclusive of existing (present day) traffic controller capabilities. First, the design specified in the ATC Controller Standard is based on the concentration of computing power in a single component (the Engine Board) that, if compatible with this standard, is interchangeable with Engine Boards designed by other manufacturers. Second, the standard provides for required and optional features, all of which are based on open standard, common protocol communication standards. Third, the ATC Controller standard is responsive to the functional requirements identified in Section 3 below. Finally, design specifications are given where needed to ensure plug-in compatibility between modular components of any ATC Controller.

Figure 1-1 provides details of the component parts of the ATC Controller and their connections.
**Figure 1-1:** Component Parts of the ATC Controller and their connections.
1.2 Key Elements Of The ATC Controller Standard

1.2.1 Form/Fit/Function

The ATC Controller provides for easy hardware upgrades in the field to adapt to newer processors, operating systems, and increased memory size and speed. It does this by requiring that each component CPU module (Engine Board) conform to a designated specific physical form and pin-out interface. Undesignated pins may, in most cases, be used for special functions selected by particular manufacturers.

While the ATC Controller packaging is ultimately left to particular manufacturers in order to allow them to be responsive to special needs, this standard describes packaging and interfaces that allow the ATC Controller to be deployed in industry standard cabinets configuration including: TS2 Type 1 & 2 cabinets, the ITS Cabinet and the 170 cabinets.

The overall ATC Controller physical design allows for either rack mount or shelf mount cabinet configurations:

- Units shall be capable of being mounting in a standard EIA 19" rack cabinet including, but not limited to, cabinets adhering to the new ITS Cabinet and the Caltrans 332 cabinet standards.
- Rack mounting hardware shall be optional for units purchased for shelf mounting but such units shall be capable of easily being retrofitted for rack mounting capability at a later date.
- All units shall be shelf mountable for operation in standard NEMA TS1, TS2 cabinet or similar configurations.
- Unit’s dimensions shall be no greater than those of the current ATC 2070.

Note that many of the design choices in this standard reflect the basic requirement that the ATC Controller provide backward interface compatibility with existing NEMA, 170, and 2070 controllers and cabinet systems.

1.2.2 Engine Board

All computational functions are concentrated on an Engine Board within the ATC Controller that meets designated minimum requirements on:

- CPU and RAM memory
- Flash memory storage
- Operating System Software
- All required serial ports
• Ethernet interface
• Standardized (form, fit and function) pin out interface
• Clock/calendar maintenance

Because the clock function is critical to the ATC Controller, details are given for minimum requirements on its ongoing accuracy. The Engine Board design includes a resident clock/calendar device and supports file transfers for the maintenance and backup of current time and date by the controller unit in the absence of AC service power. The clock/calendar device shall maintain time/date for a minimum of 30 days without AC service power applied to the controller unit and an upper bound is set on the allowable daily clock drift within the device. The ATC standard requires that when AC service power is applied to the unit, a clock pulse derived from the AC power source regularly corrects current time to prevent long term drift.

1.2.3 Communication Board

The optional Communication Board module is an internal plug-in that, if supplied, must adhere to the form, fit and electrical interface specifications of the ATC 2070 standard.

1.2.4 Front Panel

The design provides for user input through a front panel with certain required and certain optional features as follows:

Required:

• dedicated Serial port for interfacing with laptop computer, PDA, or similar device
• dedicated Ethernet port for interfacing with laptop computer, PDA or similar device
• Memory stick interface and a minimal front panel user interface for initiating bulk data transfers including required USB support

Optional: manufacturer installed front panel display and keyboard

1.2.5 Parallel and Serial I/O

To monitor the status of a variety of external field devices, the ATC Controller provides industry standard communication interfaces for asynchronous and synchronous serial communications. This standard defines a minimum of four (4) otherwise undedicated
general purpose serial communications ports for possible interface to external field devices.

This standard also requires a minimum of one dedicated synchronous serial port to interface to ITS Cabinet or TS2 Type 1 Cabinet. Optional interface modules defined in this standard include:

- serial to parallel interface module for connection to TS2 type 2 cabinet.
- serial to parallel interface module for connection to Model 170 cabinet.

1.2.6 Software interface

The ATC Controller supports the following classes of functions through a standardized Application Programming Interface (API; defined in a separate standard):

- Serial communications
- Field cabinet I/O
- Flash memory file management
- Applications task control
- Time & date management functions
- User interface support

1.3 References

1.3.1 Normative References

This standard assumes and is consistent with known versions of ATC Controller cabinet (REFERENCE WILL BE ADDED WHEN AVAILABLE) and ATC Controller API (REFERENCE WILL BE ADDED WHEN AVAILABLE) standards.

- ATC Controller Environmental Specification
- ATC Controller API Specification
- USB Specifications
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Corporation, NEC Corporation. All Rights Reserved.

http://www.usb.org/developers/docs/usbspec.zip

USB Mass Storage Overview 1.1


USB Mass Storage Bulk Only 1.0


USB Mass Storage Control/Bulk/Interrupt (CBI) Specification 1.0


USB Mass Storage UFI Command Specification 1.0


Ethernet 802.3 Specifications

IEEE 802.3-2002 Specification


1.3.2 NTCIP Standards

This standard adheres to all relevant NTCIP standards for communication protocols in
ITS devices.

1.3.3 Contact Information

Inquires, comments, and proposed or recommended revisions should be submitted to:

Standards Development Manager
Institute of Transportation Engineers
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Washington, D.C. 20005-3438 USA
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jcheeks@ite.org
2 ATC CONTROLLER CONCEPT OF OPERATIONS

This standard describes a general field located computing device that must be capable of executing applications software from various developers. Generally accepted systems engineering practices begin from user needs. This section identifies the presently known user requirements on an ATC Controller and begins to identify the associated functions. Because these users needs and applications are expected to expand in unknown ways in the future, the standard explicitly recognizes that the details of particular future applications use are not completely known at this writing. It is important nonetheless that the support and usage needs of the most commonly known and anticipated applications be defined.

As indicated above, it is the intent of this standard to describe a general purpose computing device. As such, the ATC Controller can be seen as analogous to a Personal Computer (PC). A difference between this standard and the PC is that a device meeting the ATC Controller standard must be able to withstand the harsh environment of a field located device with no special cabinet or environmental conditioning beyond that specified separately in the ATC cabinet standard (see Section 8 of this standard for details). Another difference is that the ATC Controller must be able to operate remotely in a largely unattended mode. Similar to the PC, the ATC Controller must adhere to a set of programming conventions and interfaces standards such that the applications software that runs in the device can be developed independently of the hardware and provided in a way that is consistent with the separately developed ATC API standard.

The ATC Controller must also have a high degree of reliability, be easily maintained and yet must be designed in a cost effective manner.

2.1 Problem Statement

One of the largest component costs of today’s Intelligent Transportation Systems is associated with the development, testing, deployment and maintenance of applications software. As the current trend continues towards distributing more of the intelligence of ITS out closer to the field, there is an increasing demand for more and more capable field deployable devices. This hardware must run more sophisticated applications software and operate in modern networking environments. The ATC Controller is intended to address these needs.

The ATC Controller is intended as a next generation, “Open Systems” controller which follows the “Open Systems” lineage of the current ATC 2070 and older California/ New York Model 170 controllers. “Open Systems” in this context refers to the concept of separation of hardware from software by standardizing the interface between the two. This allows software to be developed independent of the hardware. “Open Systems” help protect an agency’s investment by guarding against premature obsolescence due to
a manufacturer’s discontinuance of a particular line of equipment or the manufacturer’s ceasing of business operations altogether. Additionally, “Open Systems” [in which hardware interfaces are generically defined and standardized and adopted by multiple manufacturers] typically increase equipment procurement competition; resulting in reduced procurement costs. Deployment, integration, and maintenance costs are also generally reduced because of the commonality and interchangeability of units between various manufacturers reducing spare inventories and technician training costs.

Another important need for “Open Systems” field controller units has to do with the occasional need for custom, specially built, applications. Sometimes the demand for a particular application or custom feature is too small, from an industry-wide standpoint, to be of much interest as a product for manufacturers. Nonetheless, a particular problem or research need may require some unique functionality. With “Open Systems”, a user can write, or have someone else write their own software to satisfy a unique set of requirements. Furthermore this can be done without special support or permissions from the hardware manufacturer.

2.2 Historical Background

Many of the design choices in this standard are based on historical trends. We include that history to provide a framework for the decisions represented in this standard. We also recognize that many legacy systems are presently deployed and that any new technology, such as that specified here, must be capable of interfacing accurately and readily within existing networks of deployed equipment. Therefore, it is appropriate to document the known characteristics of elements of the deployed network.

2.2.1 The Model 170CU

The Model 170 CU was developed in the mid-1970’s to address needs discussed above for an “Open Systems” controller for transportation applications. The Model 170 obtains its hardware / software independence by requiring, by part number specification, the use of a couple of specific integrated circuit chips (for CPU and Serial Communications functions). In addition, a memory mapped I/O scheme was defined so that software developers would know precisely where to address input and output functions regardless of who manufactured the hardware unit.

While the Model 170’s architecture has been enormously successful and achieves the desired independence of the hardware and software, the Model 170 relied heavily on specified Motorola CPU and serial communications chips (or suitable substitutes). Unfortunately, these two chips and their associated family of chips have been designated for phased-out obsolescence. The issue is further compounded by the relatively poor computational performance of the Model 170, compared to today’s controller systems. This has required applications software written for the Model 170 CU to be coded in assembly or machine language and makes it difficult to move software applications written for the Model 170’s architecture to more modern system
architectures. Also, the Model 170, without an external CPU, can also not handle the performance demands of today's modern packet based high speed communications networks. Few options currently exist for agencies heavily invested in Model 170 software/hardware architecture to preserve their investments in Model 170 applications software going forward.

2.2.2 The 2070 ATC CU

The 2070 ATC is a current generation “Open Systems” controller system and is recognized explicitly within this standard. It was originally developed by Caltrans and City of Los Angeles to address some of the shortfalls associated with the Model 170 as discussed above. Its designers tried to mitigate some of the potential parts obsolesce issues which plague the Model 170. Instead of relying on the efficiency of assembly language programming, the ATC 2070 controller unit (CU) includes the necessary resources to execute programs written in higher level programming languages such as ANSI C or C++. Such higher level language programs are more easily ported to other hardware platforms should that be necessary. The ATC 2070 CU also specifies the use of a specific Operating System (OS-9) to separate the hardware from the application software. By specifying a particular OS, fixed memory mapping of User and Field Input/Output, as done with the Model 170, is no longer necessary. The OS and associated standardized support functions take care of many of the basic execution management and scheduling tasks required by application software programs. The OS further extends the hardware/software independence through I/O and memory resource sharing capabilities. These capabilities allow multiple independent applications to be run simultaneously on a single controller unit in a multi-tasking mode. This was not the case with a Model 170.

The ATC 2070 CU standard also provides for greater subcomponent interchangeability and modularity than the Model 170. Model 2070 component modules are defined through specification such that they are interchangeable among different manufacturers. These component modules are as follows:

With the Model 170 only the Modem/Communication module and the plug-in memory card are interchangeable among different manufacturers.

On the negative side, the ATC 2070 CU specification requires that only a specified CPU chip be used in its design. The ATC 2070 CU goes further and requires that a particular commercial Operating System be used. Unfortunately, the embedded hardware and Operating Systems market place is not as large and tied to a single vendor’s concept as is the PC marketplace. As a result, longevity concerns are surfacing for the ATC 2070 related to the Operating System and CPU chip architecture selections chosen for the ATC 2070. Potential adopters are concerned that additional retrofit and software porting costs would be required should either the Operating System or the CPU utilized by the ATC 2070 be no longer available.
2.3 Functional Needs

The ATC Controller standard is particularly interested in addressing the longevity concerns surrounding the ATC 2070 CU. In particular, with the today’s accelerated pace of microprocessor technology advancements and quicker product obsolescence cycles, it is desirable not to specify any particular CPU chip set or particular OS environment as is done with the ATC 2070 standard. To achieve the greater level of CPU and OS independence from applications software, an Applications Programming Interface (API) is required. An API is a set of standardized software functions that can be used by applications for the management, control and interfaces to hardware and standard OS functions.

A separate but coordinated standards effort is defining a standardized API for ATC use. The concept is a two layer approach as shown in Figure 2.1. At the lower level, functions are provided that encapsulate and hide the implementation details of a particular OS or hardware selection. At the higher level, a set of generic functions are available that make use of the lower level functions to perform higher level user interface and management functionalities. The API separates the application program from the hardware and Operating System in such a way, to break the tie to a single Operating System or CPU chip family for the controller. The ATC Controller incorporates by reference this API standard.

![Figure 2-1: Two Layered API Architecture](image)

An additional need for the ATC Controller is improved network communication interface support. Advanced communication capabilities are becoming increasingly important for
ITS field controllers. ITS data communications networks are deploying NTCIP and Internet Protocol (IP) based data communications networks. Peer to Peer networking capabilities are also increasingly required for advanced control algorithm implementations. For such networks, Ethernet is the connection interface of choice at field controllers. Additionally, communication equipment connections are moving from the older 10Mbit/sec interface rates to a 100Mbit/sec standard. The current ATC 2070 ATC supports an integral 10 Mbit/sec interface but not the increasingly more common 100 Mbit/sec interface.

Cost effective design (or improved affordability) is also a goal, particularly for fixed and predefined ITS applications where subcomponent interchangeability is not as important and may be traded off for simplicity of design, smaller size, and/or reduced deployment costs. The ATC Controller standard aims to provide enough flexibility in form factor and packaging to allow manufacturers to offer complete families of designs all of which are application software capable and meet a minimum set of ATC Controller design standards. As is the case with Personal Computers, many different hardware configurations and designs are envisioned all which would share basic applications software and external interface compatibilities.

Finally, a further need exists for controller units meeting the standard to be field upgradeable allowing agencies to cost effectively take advantage of future CPU, serial communications, driver, and memory chip improvements without necessitating the complete change out of other controller components. Towards this end, a standardized subcomponent interface is required that defines the form, fit, and function of a circuit board with CPU, serial communications, driver and memory components (referred hereafter as the Engine Board). For further protection against obsolescence, this standard requires that Engine Boards be interchangeable between various manufacturers’ controller units.

2.4 Operational Environment

Typically, a traffic system operator interfaces to an ATC through one of three mechanisms:

- **Central computer** – this type of operation configures and manages ATC applications from a computer located at a traffic management location, such as a Traffic Management Center (TMC).

- **Local computer** – this type of operation performs the same functions as a central computer does, but uses a portable interface device (e.g., laptop, PDA, etc.) connected directly to a port of the ATC.

- ** Locally** – this type of operation uses the front panel or portable interface devices (e.g., keyboard, displays, switches) at the ATC to perform the functions of configuring and managing the ATC applications.
The connection between the central computer and the ATC runs over a telecommunications network. This can be either hard wired (cables) or wireless. The network interface at the ATC can be either a serial communications port or Ethernet port. Figure 2-2 depicts the physical architecture of the key components related to a typical ATC Controller based system run from a central location.

![Diagram of ATC System Environment]

**Figure 2-2: View of a Typical ATC System Environment**

The ATC Controller is enclosed in a field located cabinet. The ATC Controller connects to other cabinet located input/output devices (i.e. load switch racks, detector racks, etc.) through serial and or parallel connections. Cabinet input/output devices, in turn, connect to field located elements (i.e. signal head, dynamic message sign, sensors, etc.).

In practice, there are additional components in a field cabinet which support the system including power distribution equipment, monitoring devices, and terminal facilities. The exact device interfaces and cabinet configuration depends on the particular ATC Controller application and type of equipment being deployed.

As a minimum, the ATC Controller must provide the necessary interfaces to support the new ITS Cabinet standard. Additionally, the ATC Controller should provide optional interface support for common legacy cabinets including Model 170, NEMA TS1, and NEMA TS2 types.

### 2.5 Representative Usage

As previously indicated, the functionally of a deployed ATC Controller will depend on the applications software loaded into it. Typical applications to be hosted on the ATC are listed in Table 2-1.
Due to the general purpose nature of ATC Controllers, many future, but currently unanticipated, an ATC Controller may be used for other applications in the future. These expanded functions may, over time, expand the operational user needs for an ATC Controller. Nonetheless, a number of basic operational usage scenarios can be discerned from present day applications.

This section identifies and describes some of the most common “use cases” to be supported by the ATC Controller and its associated applications software. Figure 2-3 provides a top-level view of the operational features offered by a typical ATC application. The definition of each feature is provided after the presentation of the diagram. The features in this diagram are subdivided into more detailed features in the text below. For these “use cases”, a more detailed “use case” feature diagram is presented along with corresponding definitions. Section 3 then uses these definitions to organize and define the various functional requirements of an ATC Controller.
The generalized operational features of an ATC can be categorized into three major areas:

- Manage/Configure Applications
- Manage External Devices
- Facilitate ease of maintenance & future hardware and software updates

The Maintenance and Support function includes features for maintenance and update/enhancement of the controller unit’s hardware and/or software.
2.5.1 Manage/Configure Controller Applications

The various sub-features for managing and configuring software applications are shown in the following figure. The subsequent sections detail these subfeatures.

![Manage/Configure Controller Applications Subfeature Areas](image)

2.5.1.1 Install/Update Applications Software Quickly and Efficiently

This feature allows the local operator or a remote computer to install or update the application software resident on the ATC.

2.5.1.2 Install/Upgrade Operating System Quickly and Efficiently

This feature allows the local operator to install or update the Operating System software resident on the ATC.
2.5.1.3 Manage Clock / Calendar Function and Synchronize with Reliable External Source

This feature is responsible for management of a real-time clock calendar function within the ATC. It allows the operator or a remote computer to interrogate and/or update the current time and date information kept by the ATC. It is responsible for synchronizing the ATC’s Operating System’s clock to an AC power source or other suitable locally available reference to adjust for internal ATC clock drift.

2.5.1.4 Configure and Verify Parameters for a Particular Local Applications

This feature allows the operator or a remote computer to manage and update the currently operational applications data stored in the ATC.

2.5.1.5 Upload/Download Data Block(s) as needed to Transfer Files and Accommodate Bulk Transfers of new Application Databases

This feature allows an operator to remotely or locally download or upload complete data blocks or data files from another computer device. It supports the operator’s ability to do bulk transfers of complete application databases to and from the ATC.

2.5.1.6 Monitor and Verify Present Applications Status

This feature allows an operator to remotely or locally view real-time reports of current applications status. The feature, depending on the application, would allow the operator to view status indicators such as operating modes, failure status, event logs, operation algorithm outputs, etc.

2.5.1.7 Allow Operator Control Application Execution (start/stop/run time/etc.)

This feature allows the operator to manage the starting, stopping, and scheduling of one or more applications on the ATC.

2.5.1.8 Facilitate the Long Term Storage of Data for Logging and other Data Storage Applications

This feature facilitates the long storage of data for logging and other data storage applications.
2.5.2 Manage External Devices

The various sub-features for “managing external devices” are shown in the following figure. The subsequent sections detail these subfeatures.

![Figure 2-5: Manage External Devices’ Subfeature Areas](image)

2.5.2.1 Manage/Control a Variety of External Field Devices

This feature addresses the need for devices to be controlled both remotely (from a central computer) and locally (either from the controller directly or from a laptop computer connected to the controller).

2.5.2.2 Monitor the Status of a Variety of External Field Devices

This feature provides the capability for the controller to monitor device status and to use that status for local control conformation, failure diagnosis, logging and/or reporting to a local operator or remote computer.

2.5.3 Facilitate Ease of Maintenance & Future Hardware and Software Updates

The various sub-features for “facilitating ease of maintenance & future hardware and software” are shown in the following figure. The subsequent sections detail these subfeatures.
2.5.3.1 Maintain/Update Controller Hardware
This feature addresses the need for controller unit hardware to be maintained and updated as technology changes and additional functional and performance capabilities are needed.

2.5.3.2 Maintain/Update Controller Software
This feature addresses the need for controller applications software to easily be maintained, updated, or ported between different manufacturer’s hardware units.

2.5.3.3 Support Diagnostics
This feature addresses the need for the controller to support self diagnosis software.
2.6 Security

The standard does not explicitly address security issues, however, network communications interfaces have been defined with provisions for data security in mind. If individual application requirements may dictate the need, security must be addressed through the software hosted by the ATC or physically by protecting access to the ATC and its interfaces. These are outside the scope of this standard.

2.7 Modes of Operation

The features identified above were developed with these three modes of operation in mind. These modes include “standalone”, “direct” and “distributed” as described below.

The “standalone” control mode assumes that the ATC is operating in the field without remote monitoring by a central computer or master controller. In this mode, applications software is loaded into non-volatile controller memory and used to control and/or monitor externally connected devices such as gates, signals, beacons, signs, etc. Device control is based on locally stored schedule, predefined control algorithms or manual operation by person present at the controller. Device monitoring might include processing of remote sensor inputs and/or monitoring the results of the controller’s control actions. Under this mode, no communications is assumed to exist between the ATC and central computer or remote master. Local operator interactions take place through ATC front panel interface, laptop computer, or similar portable device.

The “direct” control mode assumes that a remote control center or master device directly controls the external device(s) connected to the ATC. In this mode, commands are sent from control center/master to the ATC via communications network to affect the operation of local device(s) connected to the ATC.

The “distributed” control mode is a combination of the first two. Here the local ATC applications software exercises normal control but the operation is managed and synchronized through a communication network connection with a central computer or master. Control operations may frequently be overridden remotely to meet current needs and situations.
3 ATC – Controller Functional Requirements

This Functional Requirements section follows the structure established in the Concept of Operations section and defines the Functional Requirements to be supported by the ATC Controller based on common “use cases” identified in Section 2.

Following the Concept of Operations (see Section 2), the operation of the ATC Controller has been categorized into three major areas:

- Manage/Configure Controller Applications
- Manage External Devices
- Facilitate Ease of Maintenance & Future Hardware or Software Updates

The ATC Controller is fundamentally defined as a general purpose field computing device supporting many different possible software applications. Therefore the particular functional and sub-functional requirements applicable to any particular implementation can not be fully defined here.

3.1 Manage/Configure Controller Applications

3.1.1 Installing/Updating Applications Software Quickly and Efficiently

Locally – satisfied by the following requirements:

- Front panel connected dedicated Serial port for interfacing with laptop computer, PDA or similar locally connected device with software for performing this function
- Front panel connected dedicated Ethernet port for interfacing with laptop computer, PDA or similar locally connected device with software for performing this function
- Front panel Memory stick interface and a minimal front panel user interface for initiating bulk data transfers to and from a removable memory stick device – satisfied by following requirements:
  - USB port with support for memory stick and API mechanism for memory stick file access
  - Front panel display and keyboard or a serial interface for connection to connected Laptop computer or PDA device to serve as an operator interface for initializing file transfers to and from a memory stick device when such a device is connected to USB port per above requirement
Remotely – satisfied by the following requirements:

- Separate dedicated Ethernet port for possible use to communicate with a remote computer device having the necessary software for performing this function.
- Separate dedicated Serial port for possible use to communicate with a remote computer device having the necessary software for performing this function.

### 3.1.2 Installing and Upgrading the Operating System Software

This functional requirement includes the installation and upgrade of drivers, applications programming interfaces, utilities, etc. and is performed locally and remotely according to the requirements of the preceding section.

### 3.1.3 Maintain Clock/Calendar Function and Synchronize with Reliable External Sources as needed

The clock/calendar function is supported by the following:

- This Controller shall include resident clock/calendar device to transfer files support to the maintenance and backup of current time and date by the controller unit in the absence of AC power
  - Clock/calendar device shall be capable maintain time/date for a minimum of 30 days without AC power applied to the controller unit
  - Clock/calendar device drift shall be less than +/- 1 minute per 30 days at 25°C
- Applications software executing in the controller unit shall be able to set time and date on the resident clock/calendar device to the nearest 1/10 sec via a standardized Applications Programming Interface (API)
- When AC power is applied to the unit, a clock pulse derived from AC power source shall be monitored by the operating system for use in correcting current time for long term drift.
- When AC power is present, current time/date information should be maintained by the operating system and easily accessed by controller resident application software utilizing a standardized Applications Programming Interface (API)
3.1.4 Configure and Verifying Parameter(s)

Configuration and verification of parameters for particular local applications is supported via the following design characteristics of the ATC Controller:

Locally – shall be supported by:

- Optional front panel display and keyboard(s) to support operator configuring/verifying of application parameter(s) and/or
- Dedicated serial communication port for locally connected laptop, PDA or similar device with software to support operator configuring/verifying application parameter(s) from this device

Remotely – shall be supported by:

- requirements listed above, and
- presence of Application Programming Interface supporting NTCIP transfers through remote system interface

3.1.5 Uploading/Downloading Data Block(s)

The ATC Controller supports file transfers and accommodates bulk transfers of new application databases

Locally – supported by Communication port for interface to locally connected laptop, PDA or similar device with necessary software to support operator configuring/verifying application parameter(s) from this device

Remotely – supported by:

- requirements listed above, and
- presence of Application Programming Interface supporting NTCIP transfers through remote system interface

3.1.6 Monitoring and Verifying Present Application Status

The ATC Controller monitors system health overall as well as internal parameters related to particular application such as operating modes, event logs, device failures, algorithm results, etc.
Locally – supported by Communication ports (as listed in the local option of section 3.1.5 above) for interface to locally connected laptop, PDA or similar device with necessary software to support operator monitor and verifying of present applications status from this device.

Remotely – supported by:
- requirements listed above, and
- presence of Application Programming Interface supporting NTCIP transfers through remote system interfaces.

### 3.1.7 Allowing Operator Control of Application(s)

The ATC Controller allows operator control of start/stop/run times of all applications.

Locally – supported by:
- Communication ports (as listed in 3.1.a.i above) for interface to locally connected laptop, PDA or similar device with necessary software to support operator to control application control (start/stop/run time/etc.)
- Application Programming Interface allowing controller resident operator interface software to control other applications tasks (start/stop/run time/etc.)

Remotely – not supported

### 3.1.8 Facilitate the Long Term Retention of Data

The ATC Controller facilitates long term data logging and other local data storage applications via:
- flash memory for applications to store data
- API supported flash memory file management system

### 3.2 Manage External Devices

#### 3.2.1 Monitor the Status of a Variety of External Field Devices
The ATC Controller must constantly monitor the status of a variety of external field devices. In support of this, this standard describes required interfaces to provide standardized communication with external devices via industry standard asynchronous and synchronous serial communications connections.

Within this standard, this is supported by a minimum of four (4) otherwise undedicated general purpose serial communications ports for possible interface to external field devices:

- each port shall support asynchronous and synchronous communications
- each port shall support a range of baud rates up to and including 56kb/sec asynchronous and 512kb/sec synchronous
- ports shall be configurable to RS232, RS422 or RS423 interface standards

The standard also provides details of packaging and interfaces that allow this controller to be deployed in industry standard cabinets configuration including: TS2 Type 1 & 2 cabinets, the ITS Cabinet and the 170 cabinets. (The controller must provide backward interface compatibility with existing NEMA, 170, and 2070 controllers)

A minimum of one dedicated synchronous serial port to interface to ITS Cabinet or TS2 Type 1 Cabinet (or optional interface modules described below)

Optional: serial to parallel interface module for connection to TS2 type 2 cabinet.

Optional: serial to parallel interface module for connection to Model 170 cabinet.

The Controller unit shall be packaged in a housing designed for both rack mount and shelf mount cabinet configurations.

- Units shall be capable of being mounting in a standard EIA 19” rack cabinet including, but not limited to, cabinets adhering to the new ITS Cabinet and the Caltrans 332 cabinet standards.
- Rack mounting hardware shall be optional for units purchased for shelf mounting but such units shall be capable of easily being retrofitted for rack mounting capability at a later date.
- All units shall be shelf mountable for operation in standard NEMA TS1, TS2 cabinet or similar configurations.
- Unit’s dimensions shall be no greater than those of the current ATC 2070.

3.2.2 Manage/Control a Variety of External Field Devices -

This function is similar to monitoring the status of external field devices, described in Section 3.2.1 above.
3.3 Facilitate Ease of Maintenance & Future Hardware or Software Updates

3.3.1 Provide support for a standardized Application Programming Interface (API)

The ATC Controller facilitates the porting of applications software between different CPU and operating systems combinations through its support of an API (standard for the API is under development separately from this standard). It is understood that the API shall support, as a minimum the following classes of functions:

- Serial communications
- Field cabinet I/O
- Flash memory file management
- Applications task control
- Time & date management functions
- User interface support

3.3.2 Provide a Platform that allows easy field Hardware Upgrades

A goal of the ATC Controller is to readily adapt to newer processors, operating systems, and increased memory size and speed. This requires an Engine Board with:

- CPU and RAM memory
- Flash memory storage
- Operating System Software
- All required serial ports
- Ethernet interface
- Standardized (form, fit and function) pin out interface

The ATC Controller CU shall optionally include a plug-in internal Communication Board module(s) adhering to:
1. Standardized interface (form, fit, and function) established such that the Communication Boards of various manufacturers shall operate properly when installed within another manufacturer's unit.

2. If a Communications Board slot(s) is provided, slot(s) shall support current Communication Boards modules that adhere to the form, fit and electrical interface specifications of the ATC 2070 standard.
4 Engine Board Details

4.1 General Information

4.1.1 Engine Board

The Engine Board is the heart of an ATC Controller. The ATC Controller’s processor, all memory devices, serial interface devices and processor housekeeping circuits will be located on the Engine Board, which will be interchangeable between manufacturers. The plug-in form factor and standardized connectorization of the Engine Board allow it to fit into a wide variety of host controllers to suit any particular application.

The Engine Board is designed as a modular unit with the following features and characteristics:

- permits uniqueness of overall ATC Controller hardware design while maintaining software compatibility and portability
- provides a cost-effective migration path for future capability expansion
- provides for interchangeability and innovation between manufacturers
- facilitates customization of an ATC Controller for particular applications

The Engine Board dramatically simplifies future updates of the processor, operating system, memory and other core elements of the ATC Controller.

These specifications for the Engine Board require a minimum level of real-time processing capability. Suitable software will also be specified in order to determine whether a proposed Engine Board meets the minimum requirements. Manufacturers are free to add additional capabilities to their Engine Board designs so long as said functionality does not conflict with this specification in any way.

Guidance: There has been much discussion and debate regarding the approach taken in this document regarding the ATC Controller Engine Board, in particular the obvious ties to the ATC-2070. The consensus of the Project Team from the beginning has been that this work should represent an evolution of that design, rather than a revolutionary new design, and should build upon and enhance the strengths of that design while addressing the shortcomings which prevent the ATC-2070 from adequately meeting current and future requirements as outlined in this document.

The following concepts were the fundamental basis upon which the functional and design requirements specified herein for the Engine Board have been established:

- Build on the CPU platform already specified by the ATC-2070.
• Encapsulate the CPU-specific elements (processor/support hardware/OS) into a modular form which will provide a reliable migration path for future performance and obsolescence upgrades.
• Update existing features of the CPU functionality to make better use of current technology.
• Selectively add new features, which may now be available through advancements in technology, only where said features are necessary in order to meet designated functional requirements.
• Reference the upcoming ATC API for much of the detailed operational requirements.

4.1.2 Engine Board Host

The Engine Board Host shall provide the mechanical and electrical interface to the Engine Board, and is responsible for providing sufficient power and interface paths as required by this specification. With the exception of these requirements, which are detailed in this specification, manufacturers are free to construct virtually any type and form of ATC Controller host to meet any specific market need.

4.2 Mechanical and Physical

4.2.1 Board Dimensions and Mechanical Requirements

The maximum horizontal dimensions of the Engine Board shall be 5.00” L x 4.00” W. The nominal thickness of the PCB material shall be 0.062”.

The Engine Board shall have two interface connectors and four standoff holes, which shall be located as illustrated in Figure 4-1. Each connector shall have fifty pins, numbered 1-50, beginning with pin number 1 as the upper left-hand pin on each connector and with pin numbers increasing left-to-right and top-to-bottom. Standoff holes shall be 0.125” +0.010”/-0” in diameter. A 0.250” keepout area for circuit traces and components, concentric with each standoff hole, must be observed. Standoffs and/or captive fasteners are not required to be used, however the Engine Board must meet all environmental specifications regarding vibration and shock utilizing the manufacturer's standard mounting technique.

A vertical stackup diagram, showing the Engine Board and its relationship to the Host Module, is shown in Figure 4-2. Components may be placed on either side of the printed circuit board (PCB). Component height, with the exception of the interface connectors, shall not exceed 0.100” on the bottom (connector side) of the PCB and shall not exceed 0.930” on the top side of the PCB.
Figure 4-1: Engine Board Top View
4.2.2 Connector Pinout and Signal Names

The Engine Board shall have two connectors, designated P1 and P2, which are mounted on the bottom of the PCB. These connectors shall be dual-row, low-profile headers with the following specifications:

- distance post-to-post, same row: 0.100" nominal
- distance post-to-post, between rows: 0.100" nominal
- post size: 0.025" sq. nominal
- insulator thickness: 0.060" +/- 20%
- post length: 0.280" minimum, 0.350" maximum
- tail length (through PCB): 0.100" minimum, 0.150" maximum
- post plating: gold, 10u" minimum
- representative part: Samtec MTLW-125-07-G-D-07

Table 4-1 lists the connector pinouts and signal names. All name designations are from the perspective of the Engine Board (for example, TXD means data transmitted by the Engine Board).
### Table 4-1: Connector Pinout and Signal Names

<table>
<thead>
<tr>
<th>Connector P1</th>
<th>Connector P2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 VPRIMARY</td>
<td>1 VSTANDBY_5</td>
</tr>
<tr>
<td>2 VPRIMARY</td>
<td>2 VSTANDBY_3</td>
</tr>
<tr>
<td>3 VPRIMARY</td>
<td>3 RESERVED</td>
</tr>
<tr>
<td>4 VPRIMARY</td>
<td>4 RESERVED</td>
</tr>
<tr>
<td>5 GROUND</td>
<td>5 SP2_TXD</td>
</tr>
<tr>
<td>6 GROUND</td>
<td>6 SP2_RXD</td>
</tr>
<tr>
<td>7 GROUND</td>
<td>7 SP2_RTS</td>
</tr>
<tr>
<td>8 GROUND</td>
<td>8 SP2_CTS</td>
</tr>
<tr>
<td>9 SP1_TXD</td>
<td>9 SP2_CD</td>
</tr>
<tr>
<td>10 SP1_RXD</td>
<td>10 SP2_TXC_INT</td>
</tr>
<tr>
<td>11 SP1_RTS</td>
<td>11 SP2_TXC_EXT</td>
</tr>
<tr>
<td>12 SP1_CTS</td>
<td>12 SP2_RXC_EXT</td>
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<td>13 SP1_CD</td>
<td>13 SP5_TXD</td>
</tr>
<tr>
<td>14 SP1_TXC_INT</td>
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</tr>
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<tr>
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<td>17 KEYING_PIN</td>
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<tr>
<td>18 SP3_RXD</td>
<td>18 RESERVED</td>
</tr>
<tr>
<td>19 SP3_RTS</td>
<td>19 USB_DPLUS</td>
</tr>
<tr>
<td>20 SP3_CTS</td>
<td>20 USB_DMINUS</td>
</tr>
<tr>
<td>21 SP3_CD</td>
<td>21 SP8_TXD</td>
</tr>
<tr>
<td>22 SP3_TXC_INT</td>
<td>22 SP8_RXD</td>
</tr>
<tr>
<td>23 SP3_TXC_EXT</td>
<td>23 SP8_RTS</td>
</tr>
<tr>
<td>24 SP3_RXC_EXT</td>
<td>24 SP8_CTS</td>
</tr>
<tr>
<td>25 SP4_TXD</td>
<td>25 SP8_CD</td>
</tr>
<tr>
<td>26 SP4_RXD</td>
<td>26 SP8_TXC_INT</td>
</tr>
<tr>
<td>27 SP6_TXD</td>
<td>27 SP8_RXC_EXT</td>
</tr>
<tr>
<td>28 SP6_RXD</td>
<td>28 CPU_RESET</td>
</tr>
<tr>
<td>29 CPU_ACTIVE</td>
<td>29 LINESYNC</td>
</tr>
<tr>
<td>30 ENET1_TX_POS</td>
<td>30 POWERDOWN</td>
</tr>
<tr>
<td>31 ENET1_TX_NEG</td>
<td>31 POWERUP</td>
</tr>
<tr>
<td>32 ENET1_RX_POS</td>
<td>32 SPI_MOSI</td>
</tr>
<tr>
<td>33 ENET1_RX_NEG</td>
<td>33 SPI_MISO</td>
</tr>
<tr>
<td>34 RESERVED</td>
<td>34 SPI_CLK</td>
</tr>
<tr>
<td>35 RESERVED</td>
<td>35 SPI_SEL_1</td>
</tr>
<tr>
<td>36 RESERVED</td>
<td>36 SPI_SEL_2</td>
</tr>
<tr>
<td>37 RESERVED</td>
<td>37 SPI_SEL_3</td>
</tr>
<tr>
<td>38 RESERVED</td>
<td>38 SPI_SEL_4</td>
</tr>
<tr>
<td>39 ENET2_TX_POS</td>
<td>39 DKEY_PRESENT</td>
</tr>
<tr>
<td>40 ENET2_TX_NEG</td>
<td>40 RESERVED</td>
</tr>
</tbody>
</table>
### 4.2.3 Environmental Requirements

Engine boards must meet all ATC Controller environmental requirements per the ATC Controller Environmental Specification. Testing shall be performed with the Engine Board mounted in a suitable host controller assembly. The Engine Board shall be mounted using the same construction and retention devices used in the manufacturer's normal production.

### 4.3 On-Board Resources

#### 4.3.1 Central Processing Unit

The Engine Board shall incorporate a Central Processing Unit and support circuitry that shall have a minimum computational capability of 200 MIPS calculated using the Dhrystone v2.1 benchmark at 25°C.

*Guidance: This benchmark is intended only to specify a general level of performance for the controller CPU. It is understood that this benchmark alone does not completely characterize the overall performance of the controller in its normal application.*

#### 4.3.2 Startup Considerations

The Engine Board low-level hardware and operating system software initialization shall be completed, all traffic control application software will be loaded, executing and in
control of unit hardware (i.e., driving signal outputs) within a maximum of 5.0 seconds from the external application of power to the controller.

The Engine Board shall provide circuitry to prevent writing to the SRAM area and to keep the processor in a RESET state any time that VPRIMARY is less than the minimum-specified operating voltage regardless of the state of the POWERUP or POWERDOWN signals.

### 4.3.3 Memory

**FLASH Memory**

The Engine Board shall provide solid-state, permanent non-volatile memory (FLASH) for the storage of operating system software and user application programs. A minimum of 6MB of FLASH memory shall be provided for use by application programs. FLASH devices shall use a segmented architecture allowing erasing, writing and reading of individual segments. Access to this memory shall be accomplished with wait states totaling no more than 100nS. Any width of FLASH memory is acceptable, subject to any and all other performance requirements herein.

**RAM Memory**

**Dynamic RAM (DRAM)**

The Engine Board shall contain a minimum of 16MB of DRAM or equivalent volatile memory for program execution. This memory shall be organized in the native word length of the Engine Board processor for maximum performance and shall operate with zero wait states.

**Static RAM (SRAM)**

The Engine Board shall contain a minimum of 1MB of SRAM memory for non-volatile parameter storage. Access to this memory shall be accomplished with wait states totaling no more than 100nS. In the absence of primary Engine Board power VPRIMARY the SRAM shall be supported and maintained by one of the standby power sources VSTANDBY_5 or VSTANDBY_3. Current drawn from the standby power source shall not exceed 200 uA at 25°C.

### 4.3.4 Real-Time Clock (RTC)

A software-settable, hardware Real-Time Clock (RTC) shall be provided. The clock shall track seconds, minutes, hours, day of month, month and year. In the absence of primary
Engine Board power VPRIMARY the RTC shall operate from one of the standby power sources VSTANDBY_5 or VSTANDBY_3 and shall maintain an accuracy of +/−0.005% per 30 days at 25°C. Current drawn from the standby power source shall not exceed 25 uA at 25°C.

Guidance: It is expected and understood that the controller's RTC and internal software clock will need to be periodically resynchronized with an external source, either via system communications or by a local WWVB or GPS receiver connected serially.

4.3.5 ATC Controller API Support

The ATC Controller API Specification provides for a standardized Application Programming Interface (API) in support of all hardware features and functionality of the Engine Board as well as other controller components and modules. All Engine Board components, including but not limited to the processor, all memory components and support circuitry, must be capable of providing the required functionality in its entirety as defined by the ATC Controller API.

4.4 Electrical Interface

4.4.1 Power

Operating Voltages and Currents

Primary power shall be applied to the Engine Board between the VPRIMARY and GROUND interface pins. The Engine Board shall be capable of operation from any supply voltage ranging from +4.8VDC to +5.2VDC on the VPRIMARY supply. The power requirement shall not exceed 10.0 Watts from the VPRIMARY supply.

All Engine Board interface pins defined as logic-level inputs must be 5V tolerant.

Any additional voltages required for normal operation by the Engine Board, such as 3.3VDC, shall be derived from primary power VPRIMARY by circuitry located on the Engine Board.

The Engine Board is not required to provide standby power in support of the SRAM or RTC. In the absence of primary Engine Board power VPRIMARY these components shall be supported and maintained by one of the standby power sources VSTANDBY_5 or VSTANDBY_3 provided by the Engine Board Host interface. VSTANDBY_5 shall provide standby power to the Engine Board at 5.0VDC ± 10%. VSTANDBY_3 shall provide standby power at 3.3VDC ± 10%. A total of 225 uA may be drawn from both standby sources. VSTANDBY_5 and VSTANDBY_3 may be sourced from the same
backup power storage device on the host interface, and the total current requirement is considered to be shared between the two sources.

**PCB Layout Considerations**

The Engine Board connectorization provides point-source introduction of power and ground from the ATC Controller host in order to minimize power and ground loops. The Engine Board PCB layout shall be performed in such a manner so as to provide the most reliable and robust power distribution possible to the individual board components. Individual power and ground planes shall be provided for VPRIMARY and GROUND. No signal traces, other than VPRIMARY and GROUND, shall appear on these two plane layers. At least 90uF of low-ESR bulk capacitance shall be provided on the Engine Board across VPRIMARY and GROUND. Despiking capacitors across VPRIMARY and GROUND shall be used liberally, particularly adjacent to those components which operate at or near the processor's bus speed.

**Power Interruption and Restoration**

The Engine Board must properly interpret and respond to power control signals provided by the ATC Controller host, specifically the POWERUP and POWERDOWN signals. A diagram of these signals and their states under various operational conditions is shown in Figure 4-3.
Figure 4-3  Power Failure And Recovery (not to scale)
The Engine Board shall provide circuitry to prevent writing to the SRAM area and to keep the processor in a RESET state any time that VPRIMARY is less than the minimum-specified operating voltage regardless of the state of the POWERUP and POWERDOWN signals.

**POWERUP**

POWERUP is a logic-level input signal to the Engine Board. This input signal is normally in the HIGH state following a controller cold start and during normal operation. A HIGH-to-LOW transition, while the POWERDOWN signal is also in the LOW state, indicates to the Engine Board that a cold restart is to be performed. This condition is considered a long power outage. A HIGH-to-LOW transition while the POWERDOWN signal is in the HIGH state should be ignored.

**POWERDOWN**

POWERDOWN is a logic-level input signal to the Engine Board. This input signal is normally in the HIGH state following a controller cold start and during normal operation. A HIGH-to-LOW transition indicates to the Engine Board that AC power to the controller has been lost. This signal serves as an advance warning of an impending power failure, and can be used to trigger data storage or other pre-shutdown activities. Should the POWERDOWN signal transition from LOW-to-HIGH with the POWERUP signal in the HIGH state, the Engine Board application software shall continue operating normally without a restart. This condition is considered a short power outage.

### 4.4.2 Synchronization

**LINESYNC**

The LINESYNC signal is an input to the Engine Board and provides a 50% duty cycle square-wave at 60Hz. This signal is at logic-level between VPRIMARY and GROUND, and is used to provide a periodic interrupt to the Engine Board processor for use as a system tick reference. This signal must be monitored and used according to the requirements defined by the ATC Controller API.

### 4.4.3 Serial Interface Ports

**Serial Communications Interface Ports**

The Engine Board shall provide seven serial communications ports. These ports are described below. Each port shall be capable of operating at a completely independent bit rate from all other ports. Default bit rates are indicated by (*). All interface pins shall be at logic-levels. Input pins are indicated by (I), output pins by (O).
Serial Port 1 (SP1)

Principal Usage: general-purpose
Operating Modes: ASYNC / SYNC / HDLC / SDLC
Asynchronous Rates (bps): (*)1200 / 2400 / 4800 / 9600 / 19.2k / 38.4k / 57.6k / 115.2k
Synchronous Rates (bps): (*)19.2k / 38.4k / 57.6k / 76.8k / 76.8k / 153.6k
Interface Pins:
SP1_TXD: Transmit Data (O)
SP1_RXD: Receive Data (I)
SP1_RTS: Request To Send (O)
SP1_CTS: Clear To Send (I)
SP1_CD: Carrier Detect (I)
SP1_TXC_INT: Transmit Clock Internal (O)
SP1_TXC_EXT: Transmit Clock External (I)
SP1_RXC_EXT: Receive Clock External (I)

Serial Port 2 (SP2)

Principal Usage: general-purpose
Operating Modes: ASYNC / SYNC / HDLC / SDLC
Asynchronous Rates (bps): (*)1200 / 2400 / 4800 / 9600 / 19.2k / 38.4k / 57.6k / 115.2k
Synchronous Rates (bps): 153.6k / (*)614.4k
Interface Pins:
SP2_TXD: Transmit Data (O)
SP2_RXD: Receive Data (I)
SP2_RTS: Request To Send (O)
SP2_CTS: Clear To Send (I)
SP2_CD: Carrier Detect (I)
SP2_TXC_INT: Transmit Clock Internal (O)
SP2_TXC_EXT: Transmit Clock External (I)
SP2_RXC_EXT: Receive Clock External (I)

Serial Port 3 (SP3)

Principal Usage: in-cabinet communications
Operating Modes: ASYNC / SYNC / HDLC / SDLC
Asynchronous Rates (bps): (*)1200 / 2400 / 4800 / 9600 / 19.2k / 38.4k / 57.6k / 115.2k
Synchronous Rates (bps): 153.6k / (*)614.4k
Interface Pins:
SP3_TXD: Transmit Data (O)
SP3_RXD: Receive Data (I)
SP3_RTS: Request To Send (O)
SP3_CTS: Clear To Send (I)
SP3_CD: Carrier Detect (I)
SP3_TXC_INT: Transmit Clock Internal (O)
SP3_TXC_EXT: Transmit Clock External (I)
SP3_RXC_EXT: Receive Clock External (I)
Serial Port 4 (SP4)

Principal Usage: external user-interface (console)
Operating Modes: ASYNC
Asynchronous Rates (bps): 1200 / 2400 / 4800 / (*)9600 / 19.2k / 38.4k / 57.6k / 115.2k
Interface Pins: SP4_TXD: Transmit Data (O)
                SP4_RXD: Receive Data (I)

Serial Port 5 (SP5)

Principal Usage: SDLC to FIO and/or in-cabinet devices
Operating Modes: SYNC / HDLC / SDLC
Synchronous Rates (bps): 153.6k / (*)614.4k
Interface Pins: SP5_TXD: Transmit Data (O)
                SP5_RXD: Receive Data (I)
                SP5_TXC_INT: Transmit Clock Internal (O)
                SP5_RXC_EXT: Receive Clock External (I)

Serial Port 6 (SP6)

Principal Usage: front panel user-interface
Operating Modes: ASYNC
Asynchronous Rates (bps): 1200 / 2400 / 4800 / 9600 / 19.2k / (*)38.4k / 57.6k / 115.2k
Interface Pins: SP6_TXD: Transmit Data (O)
                SP6_RXD: Receive Data (I)

Serial Port 7 (SP7)

Principal Usage: general-purpose
Operating Modes: ASYNC / SYNC / HDLC / SDLC
Asynchronous Rates (bps): (*)1200 / 2400 / 4800 / 9600 / 19.2k / 38.4k / 57.6k / 115.2k
Synchronous Rates (bps): (*)19.2k / 38.4k / 57.6k / 76.8k / 76.8k / 153.6k
Interface Pins: SP8_TXD: Transmit Data (O)
                SP8_RXD: Receive Data (I)
                SP8_RTS: Request To Send (O)
                SP8_CTS: Clear To Send (I)
                SP8_CD: Carrier Detect (I)
                SP8_TXC_INT: Transmit Clock Internal (O)
                SP8_RXC_EXT: Receive Clock External (I)

Serial Peripheral Interface Port
The Engine Board shall provide a synchronous Serial Peripheral Interface Port. All SPI interface pins shall be at logic-levels. Input pins are indicated by (I), output pins by (O).

The implementation of SPI_SEL_1 is required to support DataKey operations. The implementation of SPI_SEL_2 is required to support a Host Module serial EEPROM device containing controller configuration information. SPI_SEL_3 and SPI_SEL_4 are currently unimplemented and are reserved for future SPI-related expansion.

**Serial Peripheral Interface (SPI)**

- **Principal Usage:** DataKey interface
- **Operating Modes:** SYNC
- **Synchronous Rates (bps):** (application-specific)
- **Interface Pins:**
  - SPI_MOSI: Master-Out-Slave-In (O)
  - SPI_MISO: Master-In-Slave-Out (I)
  - SPI_CLK: Clock (O)
  - SPI_SEL_1: Select 1 (O)
  - SPI_SEL_2: Select 2 (O)
  - SPI_SEL_3: Select 3 (O)
  - SPI_SEL_4: Select 4 (O)

**Universal Serial Bus (USB) Port**

The Engine Board shall provide a Universal Serial Bus (USB) port. The purpose of this port is to provide a simpler alternative to a laptop for field use by service technicians. This port will facilitate the transfer of large data files to and from the controller through the use of USB-based FLASH memory devices.

The following minimum requirements for this port have been established:

- The USB port, as a minimum, shall conform to the appropriate sections of the USB v1.1 specification for both hardware and software operation in order to support the required file transfer operations. USB v2.0 support is not required, but may be provided.

- To facilitate the transfer of files between dissimilar equipment, all USB memory devices shall be capable of being formatted using the FAT16 file system. This provides for a maximum per-device storage capacity of 2GB (assuming 32kB clusters).

Specific operational requirements for file transfers via the USB port shall be dictated by the ATC Controller API Specification.

- **Interface Pins:**
  - USB_DPLUS: Data Line Positive (I/O)
  - USB_DMINUS: Data Line Negative (I/O)

**Ethernet Port**
The Engine Board shall provide two 10BASE-T Ethernet ports which fully conform to the applicable requirements of IEEE 802.3-2002. Each port must have a unique 48-bit MAC address. All components necessary to produce the Ethernet physical layer (PHY) for each port, including the magnetic interface module, shall be located on the Engine Board.

Guidance: Independent hubs for each Ethernet port on the Host Module will provide auto-switching capability in support of both 10BASE-T and 100BASE-T external to the controller.
Ethernet Interface (ENET)

- Principal Usage: local and network communications
- Operating Mode: synchronous, Manchester-encoded, differential
- Synchronous Rates (bps): 10M
- Interface Pins:
  - ENET1_TX_POS: Port 1 Transmit Data Positive (O)
  - ENET1_TX_NEG: Port 1 Transmit Data Negative (O)
  - ENET1_RX_POS: Port 1 Receive Data Positive (I)
  - ENET1_RX_NEG: Port 1 Receive Data Negative (I)

4.4.4 Programming/Test Port

A manufacturer-specific programming and test port shall be provided on the Engine Board. Interface pins available for this purpose are designated PROG_TEST. This port (or ports) may be used for programming and testing of any on-board device(s). Examples of this test port include JTAG, BDM, Boundary-Scan, custom CPLD programming, and proprietary In-Circuit FLASH programming. Manufacturers are free to designate these pins for these purposes in any configuration on special Engine Board test adapter hosts, however all mating PROG_TEST pins on normal ATC Controller hosts shall be no-connects.

Manufacturers are also free to place proprietary programming and test connectors directly on the Engine Board, subject to the component placement height restrictions in Section 4.2.1.

4.4.5 Miscellaneous

CPU_RESET

CPU_RESET is an active-low, logic-level output signal generated by the Engine Board. This signal shall be provided to reset other system devices and shall be accessible to application programs through the ATC-API.

CPU_ACTIVE

CPU_ACTIVE is an active-low, logic-level output signal generated by the Engine Board. This signal shall be provided to indicate an active Engine Board processor and shall be accessible to application programs through the ATC-API. A typical use for this signal is to drive a front-panel 'active' or 'health' LED.

DKEY_PRESENT
DKEY_PRESENT is an active-low, logic-level input signal to the Engine Board. When this signal is active, it indicates the physical presence of a key in the DataKey receptacle.

KEYING_PIN

The interface pin designated KEYING_PIN is used to prevent incorrect insertion of the Engine Board into the host and is to be completely removed from its connector on the Engine Board.

RESERVED

All pins marked as RESERVED are reserved for future enhancements to the Engine Board specification and are not to be used for any purpose. They shall be no-connects on both Engine Boards and Engine Board Hosts.
5 Communication Interface Details

5.1 General Description

The Communications Interface performs the signal conditioning needed to adapt the ATC serial I/O to various transmission media, such as phone lines, radio and optical fiber.

This Communications Interface Specification Section includes the following:

- Transmission Media
- Modulation and Demodulation
- Mechanical Form Factor

This Communications Interface Specification Section does not include the following:

- Bit Rate Generation
- Data Content
- Error Detection and Indication

This Communications Interface Specification allows the design and manufacture of hundreds of different varieties of communications modules, interchangeable among vendors. To meet this specification, a Communications Interface shall comply with:

- Mechanical dimensions and ATC connector of this specification
- Front panel connectors of this specification
- Modulation methods of this specification
5.1.1 Interchangeability Control

1. ATC shall provide a minimum of one interchangeable communications interface.
2. Interchangeable communications interface modules are optional, not required.
3. If used, interchangeable communications interface modules shall conform to this specification, including dimensions and pin assignments.
4. Communications interfaces embedded inside the ATC need not conform to the mechanical dimensions shown here, but connectors and pin assignments shall conform to this specification.
5.1.2 Serial Port Identification

Each Communications Interface Module may use one or more serial ATC Serial Ports. For clarity, each front panel connector of the Communications Interface shall identify the connected port. Each front panel serial port legend shall exactly match that listed in the Engine Board section of this specification. For example, a 9-pin EIA-232 connector to Serial Port 1 shall be labeled “SP1” on the front panel. If the front panel connector can be assigned to different serial ports, the front panel legend shall indicate such. For example, if a 9-pin EIA-232 front panel connector can be assigned to SP1 or SP2 via a program switch, the program switch shall also illuminate either an SP1 or SP2 LED.

5.2 Mechanical Description

5.2.1 Mechanical Outline Dimensions

The ATC Communications Interface uses the 2070 ATC A2 slot mechanical form factor and pin configuration. The mechanical dimensions are as follows:

![Figure 5-2: Mechanical Dimensions](image)
### 5.2.2 ATC Connector Mechanical Pin Assignments

<table>
<thead>
<tr>
<th>PIN</th>
<th>ROW A</th>
<th>ROW B</th>
<th>ROW C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SP1TXD+</td>
<td>SP6TXD+</td>
<td>SP5TXD+</td>
</tr>
<tr>
<td>2</td>
<td>SP1TXD-</td>
<td>SP6TXD-</td>
<td>SP5TXD-</td>
</tr>
<tr>
<td>3</td>
<td>SP1RXD+</td>
<td>SP6RXD+</td>
<td>SP5TXC+</td>
</tr>
<tr>
<td>4</td>
<td>SP1RXD-</td>
<td>SP6RXD-</td>
<td>SP5TXC-</td>
</tr>
<tr>
<td>5</td>
<td>SP1RTS+</td>
<td>SP1TXC0+</td>
<td>SP5RXD+</td>
</tr>
<tr>
<td>6</td>
<td>SP1RTS-</td>
<td>SP1TXC0-</td>
<td>SP5RXD-</td>
</tr>
<tr>
<td>7</td>
<td>SP1CTS+</td>
<td>SP1TXC1+</td>
<td>SP5RXC+</td>
</tr>
<tr>
<td>8</td>
<td>SP1CTS-</td>
<td>SP1TXC1-</td>
<td>SP5RXC-</td>
</tr>
<tr>
<td>9</td>
<td>SP1DCD+</td>
<td>SP1RXC+</td>
<td>SP3TXD+</td>
</tr>
<tr>
<td>10</td>
<td>SP1DCD-</td>
<td>SP1RXC-</td>
<td>SP3TXD-</td>
</tr>
<tr>
<td>11</td>
<td>SP2TXD+</td>
<td>SP4TXD+</td>
<td>SP3RXD+</td>
</tr>
<tr>
<td>12</td>
<td>SP2TXD-</td>
<td>SP4TXD-</td>
<td>SP3RXD-</td>
</tr>
<tr>
<td>13</td>
<td>SP2RXD+</td>
<td>SP4RXD+</td>
<td>SP3RTS+</td>
</tr>
<tr>
<td>14</td>
<td>SP2RXD-</td>
<td>SP4RXD-</td>
<td>SP3RTS-</td>
</tr>
<tr>
<td>15</td>
<td>SP2RTS+</td>
<td>SP2TXC0+</td>
<td>SP3CTS+</td>
</tr>
<tr>
<td>16</td>
<td>SP2RTS-</td>
<td>SP2TXC0-</td>
<td>SP3CTS-</td>
</tr>
<tr>
<td>17</td>
<td>SP2CTS+</td>
<td>SP2TXC1+</td>
<td>SP3DCD+</td>
</tr>
<tr>
<td>18</td>
<td>SP2CTS-</td>
<td>SP2TXC1-</td>
<td>SP3DCD-</td>
</tr>
<tr>
<td>19</td>
<td>SP2DCD+</td>
<td>SP2RXC+</td>
<td>SP3TXCO+</td>
</tr>
<tr>
<td>20</td>
<td>SP2DCD-</td>
<td>SP2RXC-</td>
<td>SP3TXCO-</td>
</tr>
<tr>
<td>21</td>
<td>DCGND1</td>
<td>NA</td>
<td>SP3TX1+</td>
</tr>
<tr>
<td>22</td>
<td>NETWK1</td>
<td>NA</td>
<td>SP3TXC1</td>
</tr>
<tr>
<td>23</td>
<td>NETWK2</td>
<td>NA</td>
<td>SP3RXC+</td>
</tr>
<tr>
<td>24</td>
<td>NA</td>
<td>LINESYNC</td>
<td>SP3RXC-</td>
</tr>
<tr>
<td>25</td>
<td>NETWK3</td>
<td>POWERUP</td>
<td>CPURESET</td>
</tr>
<tr>
<td>26</td>
<td>NETWK4</td>
<td>POWERDN</td>
<td>FPLED</td>
</tr>
<tr>
<td>27</td>
<td>DCGND1</td>
<td>DCGND1</td>
<td>DCGND1</td>
</tr>
<tr>
<td>28</td>
<td>+12 SER</td>
<td>-12 SER</td>
<td>+5 STDBY</td>
</tr>
<tr>
<td>29</td>
<td>+5 VDC</td>
<td>+5 VDC</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>30</td>
<td>DCGND1</td>
<td>DCGND1</td>
<td>DCGND1</td>
</tr>
<tr>
<td>31</td>
<td>+12 VDC</td>
<td>+12 VDC</td>
<td>+12 VDC</td>
</tr>
<tr>
<td>32</td>
<td>DCGND2</td>
<td>DCGND2</td>
<td>DCGND2</td>
</tr>
</tbody>
</table>

**Notes:**

1. Signal directions are referenced to the Engine Board, not the Communications Interface. For example, SP1TXD is Serial Port 1 data transmitted from the Engine Board to the Communications Interface. SP1RxD is Serial Port 1 data received by the Engine Board from the Communications Interface.

2. Multiple Communications Interface slots shall be identical to that shown. Output signals FROM the Engine Board are simply transmitted to all Communications Interfaces modules simultaneously. Line drivers for input signals TO the Engine Board are enabled by activity on that signal, and disabled by lack of activity for 10 bit periods.
5.2.3 Mechanical Field Connections

5.2.3.1 EIA-232 Field Connections

EIA-232 field connection to the Communications Interface shall be via a 9-pin “D” connector (sockets) mounted on the Communications Interface front panel. The pin assignments are as follows:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DCD</td>
<td>Carrier Detect</td>
<td>In</td>
</tr>
<tr>
<td>2</td>
<td>RxD</td>
<td>Received Data</td>
<td>In</td>
</tr>
<tr>
<td>3</td>
<td>TxD</td>
<td>Transmitted Data</td>
<td>Out</td>
</tr>
<tr>
<td>4</td>
<td>NA</td>
<td>Not Used</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>DC GND</td>
<td>DC Reference</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>NA</td>
<td>Not Used</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>RTS</td>
<td>Request to Send</td>
<td>Out</td>
</tr>
<tr>
<td>8</td>
<td>CTS</td>
<td>Clear to Send</td>
<td>In</td>
</tr>
<tr>
<td>9</td>
<td>NA</td>
<td>Not Used</td>
<td></td>
</tr>
</tbody>
</table>
### 5.2.3.2 EIA-485 Field Connections

EIA-485 field connections to the Communications Interface shall be via a choice of two connector arrangements:

#### 5.2.3.2.1 One EIA-485 Port

EIA-485 field connection to 2 ports shall be via a 15-pin “D” connector (sockets) mounted on the Communications Interface front panel. The pin assignments are as follows:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TxD+</td>
<td>Transmitted Data</td>
<td>Out</td>
</tr>
<tr>
<td>2</td>
<td>TxD-</td>
<td>Transmitted Data</td>
<td>Out</td>
</tr>
<tr>
<td>3</td>
<td>RxD+</td>
<td>Received Data</td>
<td>In</td>
</tr>
<tr>
<td>4</td>
<td>RxD-</td>
<td>Received Data</td>
<td>In</td>
</tr>
<tr>
<td>5</td>
<td>RTS+</td>
<td>Request to Send</td>
<td>Out</td>
</tr>
<tr>
<td>6</td>
<td>RTS-</td>
<td>Request to Send</td>
<td>Out</td>
</tr>
<tr>
<td>7</td>
<td>CTS+</td>
<td>Clear to Send</td>
<td>In</td>
</tr>
<tr>
<td>8</td>
<td>CTS-</td>
<td>Clear to Send</td>
<td>In</td>
</tr>
</tbody>
</table>

#### 5.2.3.2.2 Two EIA-485 Ports

EIA-485 field connection to 2 ports shall be via a 15-pin “D” connector (sockets) mounted on the Communications Interface front panel. The pin assignments are as follows:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TXDATA+</td>
<td>Transmitted Data</td>
<td>Out</td>
</tr>
<tr>
<td>2</td>
<td>DC GND</td>
<td>DC Reference</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>TXCLOCK+</td>
<td>Transmitter Clock</td>
<td>Out</td>
</tr>
<tr>
<td>4</td>
<td>DC GND</td>
<td>DC Reference</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>RXDATA+</td>
<td>Receiver Data</td>
<td>In</td>
</tr>
<tr>
<td>6</td>
<td>DC GND</td>
<td>DC Reference</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>RXCLOCK+</td>
<td>Receiver Clock</td>
<td>In</td>
</tr>
<tr>
<td>8</td>
<td>NA</td>
<td>Not Used</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>TXDATA-</td>
<td>Transmitted Data</td>
<td>Out</td>
</tr>
<tr>
<td>10</td>
<td>DC GND</td>
<td>DC Reference</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>TXCLOCK-</td>
<td>Transmitter Clock</td>
<td>Out</td>
</tr>
<tr>
<td>12</td>
<td>DC GND</td>
<td>DC Reference</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>RXDATA-</td>
<td>Receiver Clock</td>
<td>In</td>
</tr>
<tr>
<td>14</td>
<td>DC GND</td>
<td>DC Reference</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>RXCLOCK-</td>
<td>Receiver Clock</td>
<td>In</td>
</tr>
</tbody>
</table>
### 5.2.3.3 Private Line Modulator / Demodulator (Modem) Connections

Private phone line twisted pair field connections to the Communications Interface shall be via a choice of two connector arrangements:

#### 5.2.3.3.1 Internal and External Modem Connections

M14 AMP connector (sockets) mounted on the Communications Interface front panel. This connector includes signals for transmit twisted pair and receive twisted pair phone lines for use with internal modem, plus EIA-232 signals for use with external modem. The pin assignment is as follows:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>AUDIO IN</td>
<td>Phone Line Receive Pair</td>
<td>In (4 Wire)</td>
</tr>
<tr>
<td>B</td>
<td>AUDIO IN</td>
<td>Phone Line Receive Pair</td>
<td>In (4 Wire)</td>
</tr>
<tr>
<td>C</td>
<td>AUDIO OUT</td>
<td>Phone Line Transmit Pair</td>
<td>Out (4 Wire, I/O 2 Wire)</td>
</tr>
<tr>
<td>D</td>
<td>+5 VDC</td>
<td>Low Power +5 VDC Source</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>AUDIO OUT</td>
<td>Phone Line Transmit Pair</td>
<td>Out (4 Wire, I/O 2 Wire)</td>
</tr>
<tr>
<td>F</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>DCD</td>
<td>Carrier Detect</td>
<td>In</td>
</tr>
<tr>
<td>J</td>
<td>RTS</td>
<td>Request to Send</td>
<td>Out</td>
</tr>
<tr>
<td>K</td>
<td>TXD</td>
<td>Transmitted Data</td>
<td>Out</td>
</tr>
<tr>
<td>L</td>
<td>RxD</td>
<td>Received Data</td>
<td>In</td>
</tr>
<tr>
<td>M</td>
<td>CTS</td>
<td>Clear to Send</td>
<td>In</td>
</tr>
<tr>
<td>N</td>
<td>DC GND</td>
<td>DC Reference</td>
<td></td>
</tr>
<tr>
<td>P</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### 5.2.3.4 Internal Only Modem Connections

Nine pin “D” connector (pins) mounted to the Communications Interface front panel. This connector includes signals for transmit and receive twisted pair phone lines for use with internal modem. The pin out assignments are as follows:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>AUDIO OUT</td>
<td>Phone Line Transmit Pair</td>
<td>Out (4 Wire), I/O (2 Wire)</td>
</tr>
<tr>
<td>2</td>
<td>AUDIO OUT</td>
<td>Phone Line Transmit Pair</td>
<td>Out (4 Wire), I/O (2 Wire)</td>
</tr>
<tr>
<td>3</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>AUDIO IN</td>
<td>Phone Line Receive Pair</td>
<td>In (4 Wire Only)</td>
</tr>
<tr>
<td>5</td>
<td>AUDIO IN</td>
<td>Phone Line Receive Pair</td>
<td>In (4 Wire Only)</td>
</tr>
<tr>
<td>6</td>
<td>EQ GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>EQ GND</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5.2.3.5 Dial-Up Line Modem Connections

Private phone line twisted pair field connections to the Communications Interface shall be via a 9 pin “D” connector (pins) mounted to the Communications Interface front panel. The pin assignments are as follows:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>NA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>EQ GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>AUDIO I/O</td>
<td>Phone Line Pair</td>
<td>In / Out</td>
</tr>
<tr>
<td>8</td>
<td>AUDIO I/O</td>
<td>Phone Line Pair</td>
<td>In / Out</td>
</tr>
<tr>
<td>9</td>
<td>EQ GND</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

5.2.3.6 Single Mode Fiber Connections

Single-mode fiber field connections to the Communications Interface shall be via 1300 nM threaded FC or 1300 nM ST connector for both laser transmitters and PIN diode receivers.

5.2.3.7 Multi Mode Fiber Connections

Multi-Mode fiber connections to the Communications Interface shall be via 820 nM ST connectors for both LED transmitters and phototransistor receivers.

5.2.3.8 Wide Area Radio Connections

Wide area radio field connections to the antenna shall be via a TNC coaxial connector.

5.2.3.9 Infrared Connections

Wireless infrared field connections to an external device are via a red transparent window.

5.2.3.10 Ethernet Connections

Ethernet connections to the Communications Interface shall be via an RJ-45 modular jack, with the following pin configuration:
### COMMUNICATION INTERFACE DETAILS

#### 5.3 Operational Description

**5.3.1 Interface to ATC**

**5.3.1.1 EIA-485 Signals**

Except NETWORK1-NETWORK4 and FP LED, all signal lines of the 96-pin ATC connector shall be electrically EIA-485, balanced differential. Please refer to the EIA-485 document for electrical specifications.

The EIA-485 signals are biased by the ATC (not the Communications Interface Module) to provide the following:

- A 150 ohm resistor connected from DATA to /DATA on each simplex receiver.
- No termination resistor on each simplex transmitter
- A 150 ohm resistor connected from DATA to /DATA on each half duplex transceiver
- A 1.5K resistor from DATA to +5V and a 1.5K resistor from /DATA to DCGND1 to insure a stable state when the Communications Interface Module is not installed.

Please refer to the Communications Section for information on EIA-485 terminations.

**5.3.1.2 Ethernet Signals**

NETWORK1-NETWORK4 lines of the 96-pin ATC connector shall be 10 Base-T or 100 Base-T Ethernet. Proper selection of circuit board trace width, spacing, and shielding shall be observed for correct characteristic impedance and to prevent cross talk to adjacent signals.

**5.3.1.3 Power Signals**

DCGND1 shall be the common reference for +5 VDC, +12 SER, -12 SER and all signals.
DCGND2 shall be the common reference for +12 VDC.

5.3.1.4 Electrical Isolation

DCGND2 and +12 VDC as a group shall be electrically isolated from all other signals and power sources as a group, maintaining the isolation specifications of the Environmental Section. Eq GND shall maintain the isolation specifications of the Environmental Section.

Communications Interface field connections shall be electrically isolated from all ATC signals, power sources and EQ GND.

Field connections of the EIA-232 and EIA-485 versions of the Communications Interface shall be optically isolated using devices capable of at least 1 Mbps.

Field connections of the Ethernet, Private Line Modem and Dial-Up Modem versions of the Communications Interface shall be magnetically isolated via isolation transformers with the proper characteristic impedance.

Field connections of the Single Mode Fiber, Multi Mode Fiber and Infrared versions of the Communications Interface are inherently isolated via the non-conductive optical media.

Field connections of the Wide Area Radio version of the Communications Interface are inherently isolated via the non-conductive radio frequency media.

5.3.2 Modulation and Demodulation

5.3.2.1 EIA-232

(Guidance: This paragraph is intended to represent the present 2070-7A).

Description:

The EIA-232 versions of the Communications Interface shall convert the ATC EIA-485 signals to EIA-232 bipolar simplex, meaning each signal is unidirectional, point-to-point, without ability to disable the transmitter.

Indicators:

EIA-232 versions of the Communications Interface shall include the following indicators:

<table>
<thead>
<tr>
<th>Legend</th>
<th>Indicator Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX ON=</td>
<td>Transmitted Data at Field Wire is Positive Volts</td>
</tr>
<tr>
<td>RX ON=</td>
<td>Received Data at Field Wire is Positive Volts</td>
</tr>
</tbody>
</table>
Specifications:

Please refer to the EIA-232 specification for more detailed information on electrical specifications and signal definition.

5.3.2.2 EIA-485

(Guidance: This paragraph is intended to represent the present 2070-7B).

Description:

EIA-485 versions of the Communications Interface shall convert the ATC EIA-485 signals to isolated EIA-485, which may be simplex or half duplex.

Indicators:

EIA-485 versions of the Communications Interface shall include the following indicators:

<table>
<thead>
<tr>
<th>Front Panel</th>
<th>Indicator Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>ON=DATA at Field Wire is 0V, /DATA at Field Wire is Positive Volts</td>
</tr>
<tr>
<td>RX</td>
<td>ON=DATA at Field Wire is 0V, /DATA at Field Wire is Positive Volts</td>
</tr>
</tbody>
</table>

Specifications:

Please refer to the EIA-485 specification for more detailed information on electrical specifications and signal definition.

5.3.2.3 Private Line Modem

Description:

Private Line Modem versions of the Communications Interface shall convert the ATC EIA-485 signals to modulated audio suitable for communications on an unconditioned private phone line pair, meaning the line is direct wire not connected to a phone company.

Modulation schemes used here convert the binary “1” and binary “0” bits of the data stream into audio tones, known as the MARK and SPACE. The demodulation scheme consists of converting each of the tones back to binary “1” and binary “0” bits to replicate the original transmitted data stream at the receiving device.

When RTS is asserted by the ATC, the modem shall transmit the MARK tone for a period of time, allowing the receiving modem to lock on to the tone and assert Carrier Detect (DCD). At the end of this time period, the transmitting modem asserts Clear to Send (CTS), signaling the ATC to begin sending data. At the end of the data packet, the
ATC unasserts RTS and the transmitting modem stops sending a tone. DCD is unasserted by the receiving modem.

A front panel selector switch for each channel shall be provided to select FULL or HALF duplex operation. This scheme shall be capable of operating half-duplex on a single phone line, or full duplex on two different phone lines, one line for transmission and another line for reception, allowing simultaneous data transmission in both directions.

A second front panel selector switch for each channel shall disable the modem transmitter, in the event an ATC malfunctions with its RTS constantly asserted.

A third switch front panel shall break the power supply current to both channels, allowing the Communications Interface to be inserted into the ATC without causing a reboot or other ATC malfunction other than a normal recoverable communications error.

A fourth switch, mounted internally, shall implement anti-streaming which shall disable the modem transmitter in the event an ATC malfunctions with its RTS constantly asserted. If RTS is asserted for the specified time, the modem transmitter shall be turned OFF. The anti-streaming timer is reset if RTS is unasserted, or if TxD is active. This fourth switch allows anti-streaming to be disabled if the modem is installed in a FULL duplex central office, which continuously transmits to remote ATCs.

**Indicators:**

<table>
<thead>
<tr>
<th>Front Panel Legend</th>
<th>Indicator Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>ON= SPACE Tone at Field Wire</td>
</tr>
<tr>
<td>RX</td>
<td>ON= SPACE Tone at Field Wire</td>
</tr>
<tr>
<td>CD</td>
<td>ON= Received Tone Present</td>
</tr>
</tbody>
</table>

**Modulation Methods:**

Two different modulation methods shall be allowed under this specification as follows:

5.3.2.3.1 *Frequency Shift Keying (FSK)*, 300 to 1200 bps, 0 to 9600 bps.

(Guidance: *This paragraph is intended to represent the present 2070-6A and 2070-6B*).

FSK modulation is simply transmitting one tone for a logic “1” (MARK) and a different tone for a logic “0” (SPACE), similar to pressing two different buttons on a touchtone telephone.

Two different FSK versions shall be available, which are 300 to 1,200 bps, as well as 0 to 9,600 bps. The two versions differ in the MARK and SPACE tones. The 0 to 9,600 bps version handles a wider variety of bit rates, but it’s higher frequency tones travel shorter distances. For example, both versions transmit at the same power level and receive at the same sensitivity, but phone wire attenuates the higher frequencies of the 0
to 9600 bps version more rapidly. (Please refer to wire manufacturer’s specifications for decibels (dB) loss per mile.)

**Specifications:**

The 300 to 1200 bps and 0 to 9600 bps shall have the following common specifications:

- **Modulation:** Phase coherent frequency shift keying (FSK).
- **Data Format:** Asynchronous, serial by bit.
- **Line:** Type 3002 voice-grade, unconditioned.
- **Transmit Level:** 0 to –8 dB at 1.7 KHz, continuously adjustable
- **Sensitivity:** 0 to –40 dB
- **Receiver Filter:** 20 dB/Octave minimum active attenuation outside operating band
- **RTS to CTS Delay:** 8 to 14 mS
- **Carrier Detect:** 6 to 10 mS at MARK frequency
- **Receiver Squelch:** 5.5 to 7.5 mS
- **Soft Carrier OFF:** 8 to 12 mS
- **Recovery Time:** 22 mS maximum from Transmit to Receive
- **Error Rate:** Less than 1 bit in 100,000 bits
- **Signal to Noise:** 16 dB over 300 to Controller Hz band
- **Transmit Noise:** -50 dB maximum into 600 ohms, 300 to Controller Hz band
- **Anti-Stream Time:** 6 to 8 seconds

The 300 to 1200 bps and 0 to 9600 bps specifications differ as follows:

<table>
<thead>
<tr>
<th>Data Rate Version</th>
<th>300 to 1200 bps</th>
<th>0 to 9600 bps</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MARK Tone</strong></td>
<td>1.2 KHz</td>
<td>11.4KHz</td>
</tr>
<tr>
<td><strong>SPACE</strong></td>
<td>2.2 K Hz</td>
<td>17.6KHz</td>
</tr>
<tr>
<td><strong>Soft Carrier Freq</strong></td>
<td>900 Hz</td>
<td>7.8 KHz</td>
</tr>
</tbody>
</table>

5.3.2.3.2 **Di-Phase, 2,400 to 19,200 bps**

(Guidance: This paragraph describes a modulation/demodulation technique to replace legacy 1200 bps FSK modems on existing unconditioned phone lines. Equivalent transmission distances are achieved at 19,200 bps, without software changes. ITU “V” series modems, such as V.90 are not recommended for this application due to the excessive RTS to CTS “training” time in half-duplex polling applications such as NTCIP.)

Di-phase modulation provides two tones as well as two phases, allowing increased bit rates over FSK modulation.
Specifications:

1. Modulation: Differential Di-Phase, EUROCOM Standard D1
3. Line: Type 3002 voice-grade, unconditioned.
4. Transmit Level: 0 to –8 dB at 1.7 KHz, continuously adjustable
5. Sensitivity: 0 to –40 dB
6. Receiver Filter: 20 dB/Octave minimum active attenuation outside operating band
7. RTS to CTS Delay: 8 to 14 mS
8. Carrier Detect: 6 to 10 mS at MARK frequency
9. Receiver Squelch: 5.5 to 7.5 mS
10. Soft Carrier OFF: NA (no soft carrier)
11. Recovery Time: 22 mS maximum from Transmit to Receive
12. Error Rate: Less than 1 bit in 100,000 bits
13. Signal to Noise: 16 dB over 300 to 3000 Hz band
14. Transmit Noise: -50 dB maximum into 600 ohms, 300 to 3000 Hz band
15. Anti-Stream Time: 6 to 8 seconds

5.3.2.4 Dial Up Line Modem

(Guidance: This paragraph is intended to represent a standard dial-up modem.)

Description:

The Dial Up Modem versions of the Communications Interface shall convert the ATC EIA-485 signals to audio tones attached to public phone lines and switching equipment. The Dial Up Modem shall be capable of data transmission and reception, as well as dialing out and dialing in on a standard analog phone line.

Indicators:

Dial Up versions of the Communications Interface shall include the following indicators:

<table>
<thead>
<tr>
<th>Legend</th>
<th>Indicator Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>ON= Transmitted Data Activity</td>
</tr>
<tr>
<td>RX</td>
<td>ON= Received Data Activity</td>
</tr>
<tr>
<td>CD</td>
<td>ON= Received Tone Present</td>
</tr>
<tr>
<td>RS</td>
<td>ON= RTS Asserted</td>
</tr>
</tbody>
</table>

Specifications:

Please refer to the ITU V.90 specification for detailed information on electrical specifications and signal definition. Front Panel connector shall be RJ-11.
5.3.2.5  Single Mode Fiber

(Guidance: This paragraph is intended to represent the 2070-6D.)

Description:

The Single Mode Fiber versions of the Communications Interface shall convert the ATC EIA-485 transmitted data to laser light, and laser light to ATC EIA-485 received data. Amplitude modulation (AM) is employed, meaning that a logic “0” is transmitted at a high light amplitude (or brightness), while logic “1” is transmitted at a lower (or OFF) amplitude.

Danger: Be aware that single-mode laser light is invisible to the human eye, but is of sufficient power to cause damage. Never look directly into a laser transmitter. Always cover unused laser transmitters with opaque dust covers.

Indicators:

Single Mode Fiber versions of the Communications Interface shall include the following indicators:

<table>
<thead>
<tr>
<th>Legend</th>
<th>Indicator Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>TX ON= Transmitter is Emitting High Amplitude Light</td>
</tr>
<tr>
<td>RX</td>
<td>RX ON= Receiver is Detecting High Amplitude Light</td>
</tr>
</tbody>
</table>

Specifications:

- Optical Transmit Level: 1300 nM Single Mode Laser
- -6 to –15 dBm, Continuously Adjustable
- Receiver Sensitivity: -30 dBm
- Data Rate: 100K bps
- Transmitter Compensation: Temperature and aging

5.3.2.6  Multi Mode Fiber

(Guidance: This paragraph is intended to represent the 2070-6D.)

Description:

The Multi Mode Fiber versions of the Communications Interface shall convert the ATC EIA-485 transmitted data to light, and light to ATC EIA-485 received data. Amplitude modulation (AM) is employed, meaning that a logic “0” is transmitted at a high light amplitude (or brightness), while logic “1” is transmitted at a lower (or OFF) amplitude.
Indicators:

Multi Mode Fiber versions of the Communications Interface shall include the following indicators:

<table>
<thead>
<tr>
<th>Legend</th>
<th>Indicator Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>ON= Transmitter is Emitting High Amplitude Light</td>
</tr>
<tr>
<td>RX</td>
<td>ON= Receiver is Detecting High Amplitude Light</td>
</tr>
</tbody>
</table>

Specifications:

- Optical 820 nM Multi Mode Light Emitting Diode (LED)
- Transmit Level: -6 to –15 dBm, Continuously Adjustable
- Receiver Sensitivity -30 dBm
- Data Rate 100K bps
- Transmitter Compensation Uncompensated

5.3.2.7 Wide Area Radio

(Guidance: This paragraph is intended to represent a license-free data radio offering a good combination of distance and data integrity.)

Description:

The Wide Area Radio version of the Communications Interface shall convert the ATC EIA-485 transmitted data to RF, and RF to ATC EIA-485 received data. Spread spectrum frequency hopping is employed, meaning that the radio transmits at high power on a frequency channel, then “hops” to another channel. This insures that the average power transmitted on any one frequency is below the limit to require an FCC license.

Indicators:

Wide Area Radio versions of the Communications Interface shall include the following indicators:

<table>
<thead>
<tr>
<th>Legend</th>
<th>Indicator Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX</td>
<td>ON= Transmitted Data Activity</td>
</tr>
<tr>
<td>RX</td>
<td>ON= Received Data Activity</td>
</tr>
</tbody>
</table>
Specifications:

2. Data Transmission: Simplex, Half Duplex and Full Duplex
3. Data Rate: 1200 to 19,200 bps, Asynchronous
4. Transmitter Power: 1 Watt Maximum
5. Error Rate: Less than 1 bit in 100,000 bits

5.3.2.8 Infrared

(Guidance: This paragraph is intended to represent an interface to a standard PDA.)

Description:

The Infrared versions of the Communications Interface shall convert the ATC EIA-485 transmitted data to light and light to ATC EIA-485 received data. The light beam is infrared, meaning it is outside the visible color range detected by the human eye. The light transmission is similar to a standard television remote control, meaning that its light emission power is safe to the human eye. As with a TV remote control, the transmitting device must be used within the line of sight, aimed towards the controller red window, and located within approximately six feet.

Indicators:

None

Specifications:

1. Optical: IrDA Physical Layer Implementation
2. Modulation: 3/16 Encode / Decode
3. Data Rate: 1200 bps to 115.2K bps

5.3.2.9 Ethernet

(Guidance: This paragraph is intended to represent the 2070-1B Ethernet)

Description:

The Ethernet version of the Communications Interface shall adapt the ATC NETWORK1-4 signals. The Ethernet port may be directly tied to NETWORK1-4 or buffered as a hub.

Indicators:

Due to the higher event speeds of Ethernet, each indication shall be extended 100 mS.

Ethernet versions of the Communications Interface shall include the following indicators:
Front Panel

Legend | Indicator Function
---|---
T | ON= Transmitted Data or Received Data is logic “1”
100 | ON= 100 MBPS Data Rate

Specifications:

Please refer to IEEE 802.3 for detailed specifications.

### 5.4 Communications Interface Versions

Each version of the Communications Interface shall consist of the following:

- A printed circuit board assembly of the size and shape described in Paragraph 2.1
- A connection to the ATC serial ports and power, as described in Paragraph 2.2
- One or more communications ports described in Paragraph 2.3
- Modulation / demodulation circuitry for each port, described in Paragraph 3.

By using different combinations of ports, an unlimited number of Communications Interface versions may be configured, compliant to this specification.

The following is a list of the existing Communications Interface Versions:

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2070-6A</td>
<td>Dual 300 to 1200 bps Modem</td>
</tr>
<tr>
<td>2070-6B</td>
<td>Dual 0 to 9600 bps Modem</td>
</tr>
<tr>
<td>2070-6D</td>
<td>Fiberoptic Communications Interface</td>
</tr>
<tr>
<td>2070-7A</td>
<td>Dual EIA-232 Serial Interface</td>
</tr>
<tr>
<td>2070-7B</td>
<td>Dual EIA-485 Serial Interface</td>
</tr>
</tbody>
</table>

As new versions are defined, this list will expand.

Each version may be implemented using any of the following three design methods:

- Dedicated circuit design, each version ordered as separate vendor part numbers
- Common base board, with selectable modulation via plug-in circuit assemblies
- Common board, with selectable modulation via digital signal processor (DSP) software

Please refer to the Joint NEMA/AASHTO/ITE ATC Standard for detailed specifications of the 2070-6A, 2070-6B, 2070-7A and 2070-7B.

The Joint NEMA/AASHTO/ITE ATC Standard does not include a specification for the 2070-6D. The draft specification for the 2070-6D follows.
2070-6D Internal Fiber Modem

The 2070-6D Fiber Modem is a 1300 nM Single Mode fiberoptic transmitter and receiver. The 2070-6D provides two sets of fiber transmitter and receiver pairs that can operate as two independent serial channels (MASTER) or as a fiber repeater (REMOTE) via front panel switch selection. The 2070-6D incorporates powerful laser transmitters that provide high-speed data transmission at long distances.

2070-6D Operation

The 2070-6D Fiberoptic Converter is a printed circuit board assembly that plugs into the A2 slot of the 2070 ATC that is used to condition serial ports SP1 and SP2 for use with optical fiber, EIA-232, or EIA-485. The fiber cable attach to the 2070-6D via 1300 nM single mode fiber, FC style threaded connectors.

The 2070-6D has two front-panel switches. The MASTER/REMOTE switch selects whether the 2070-6D is installed in a Master Controller, or a Remote Controller, while the FIBER/DB9 switch enables or disables the DB9 connection to EIA-232 and EIA-485.

The 2070-6D contains internal rechargeable battery back-up circuitry that will power the fiber drivers and receivers for more than two hours after loss of controller power, preserving the integrity of the fiber link.

Operating Modes

The 2070-6D includes two 2-position front panel programming switches, resulting in four possible operating modes.

Master Mode 1: MASTER/REMOTE = MASTER, FIBER/DB9 = FIBER

This mode is used to drive two independent serial fiber links on two independent serial ports. In this mode, serial port SP1 transmits data on Emitter 1, and receives data on Detector 1. Serial port SP2 transmits data on Emitter 2, and receives data on Detector 2. In this mode, the DB9 connector is disabled.

Applications: This mode can be used to drive two separate fiber links, but is also commonly used to drive a single critical fiber ring (see Figure 5-1).
Master Mode 2: MASTER/REMOTE = MASTER, FIBER/DB9 = DB9

This mode is used to drive two fiber links simultaneously from one serial port, plus a hardwired serial link from a second serial port via the DB9 connector. In this mode, serial port SP1 transmits data simultaneously on Emitter 1 and Emitter 2. Data received on SP1 is the logical “OR” of Detector 1 and Detector 2. SP2 data is transmitted and received on the DB9 connector. The DB9 electrical characteristics conform to EIA-232 if SW1, section 1 is ON. The DB9 electrical characteristics conform to EIA-485 if SW1, section 1 is OFF.

Applications: This mode can be used when the Master Controller is located in the center of a fiber link on SP1. The second serial channel (SP2) is a general purpose EIA-232 or EIA-485 serial channel to other devices.

Remote Mode 1: MASTER/REMOTE = REMOTE, FIBER/DB9 = DB9

This mode acts as a fiber signal booster/repeater on one serial port, plus a hardwired serial link from a second serial port via the DB9 connector. In this mode, data received
on Detector 1 is received on serial port SP1 and also retransmitted simultaneously on Emitter 2. Data transmitted on Emitter 1 is the logical “OR” of data received on Detector 2 and data transmitted by SP1. Circuitry is provided to arbitrate collisions. If SP1 is already transmitting data on Emitter 1, data received on Detector 2 is locked out as long as SP1 Request to Send (RTS) is asserted. If data is already being retransmitted from Detector 2 to Emitter 1, SP1 Clear to Send (CTS) is asserted during, and for a short time after, the Detector 2 data. The duration of the CTS delay is either 1 mS or 10 mS after the end of the Detector 2 data. This delay is 1 mS if SW1, section 2 is ON. This delay is 10 mS if SW1, section 2 is OFF. The 10 mS delay is recommended for use with baud rates of 9600 or less. The 1 mS delay can be used for higher baud rates. SP2 data is transmitted and received on the DB9 connector. The DB9 electrical characteristics conform to EIA-232 if SW1, section 1 is ON. The DB9 electrical characteristics conform to EIA-485 if SW1, section 1 is OFF.

Applications: This mode is used to communicate with Remote Controllers via SP1, while boosting the optical signal to the next fiber link. The second serial channel (SP2) is a general purpose EIA-232 or EIA-485 serial channel to other devices (Figure 5-1).

Remote Mode 2: MASTER/REMOTE = REMOTE, FIBER/DB9 = FIBER

This mode is reserved for future use. The DB9, Emitters and Detectors are disabled.

Anti Streaming

Anti streaming prevents a serial channel from accidentally stalling and locking-up a serial channel. The anti streaming circuit constantly monitors the RTS output of each serial channel. If a serial channel stalls in transmit mode for seven seconds, the CTS input to that channel is unasserted, which takes that channel off-line. The anti streaming circuit continues hold CTS unasserted until RTS is unasserted, whereupon the 7-second anti streaming timer is reset. Anti streaming is enabled when SW4 section 3 is ON. Anti streaming is disabled when SW4 section 3 is OFF. Anti streaming is recommended except for long data streams, such as long uploads or downloads. Long data streams must be broken up into smaller packets if anti streaming is enabled.

Battery Back Up

The 2070-6D includes internal lithium rechargeable batteries that will power the fiber links for at least two hours upon the loss of power to the controller. The front panel includes a lamp labeled “CHARGED” which illuminates when the batteries are charged to full capacity.

Fiber Drivers

One fiber driver consists of EM1. A potentiometer is used to adjust the light output amplitude. The second fiber driver consists of EM2 and a second potentiometer, and operates in a similar fashion. Front panel lamps EM1 and EM2 are provided to indicate the state of EM1 and EM2 fiber drivers.
DANGER: NEVER LOOK INTO THE FIBER DRIVERS. THE LASER LIGHT IS INVISIBLE TO THE HUMAN EYE, BUT CAN CAUSE EYE DAMAGE. BE AWARE THAT EM1 AND EM2 CAN BE TRANSMITTING UNDER BATTERY POWER, EVEN WHEN THE CONTROLLER IS NOT POWERED, OR EVEN WHEN THE MODULE IS UNPLUGGED. FOR VISUAL STATUS, ALWAYS USE THE FRONT PANEL LAMPS, NOT THE FIBER CONNECTORS.

Fiber Receivers

One fiber receiver consists of DET1, while the second fiber receiver consists of DET2. Front panel lamps DET1 and DET2 provide visual status for each of the fiber receivers.

DB9 Communications

J1 is used for the DB9 communications. J1 is programmed by a DIP switch on the 2070-6D, to follow either EIA-232 or EIA-485 electrical standard.

Battery and Charger

All of the 2070-6D communications circuitry is powered by battery voltage to insure the fiber link remains powered. When the batteries are fully discharged, the regulator is shut down, preventing further discharge of the batteries. The 2070-6D contains a charge timer. If the battery does not fully charge within the specified time, the battery charger is turned OFF to prevent overheating.

Connectors

When programmed for EIA-232 operation, DB9 connector has the following pins:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DCD</td>
<td>Carrier Detect</td>
<td>Input</td>
</tr>
<tr>
<td>2</td>
<td>RxD</td>
<td>Received Data</td>
<td>Input</td>
</tr>
<tr>
<td>3</td>
<td>TxD</td>
<td>Transmitted Data</td>
<td>Output</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>No Connection</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>DC Ground 1</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>No Connection</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>RTS</td>
<td>Request to Send</td>
<td>Output</td>
</tr>
<tr>
<td>8</td>
<td>CTS</td>
<td>Clear to Send</td>
<td>Input</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>No Connection</td>
<td></td>
</tr>
</tbody>
</table>
When programmed for EIA-485 operation, DB9 connector has the following pin out:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Description</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TxD+</td>
<td>Transmitted Data</td>
<td>Output</td>
</tr>
<tr>
<td>2</td>
<td>TxD-</td>
<td>Transmitted Data</td>
<td>Output</td>
</tr>
<tr>
<td>3</td>
<td>RxD+</td>
<td>Received Data</td>
<td>Input</td>
</tr>
<tr>
<td>4</td>
<td>RxD-</td>
<td>Received Data</td>
<td>Input</td>
</tr>
<tr>
<td>5</td>
<td>DC Ground 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>RTS+</td>
<td>Request to Send</td>
<td>Output</td>
</tr>
<tr>
<td>7</td>
<td>RTS-</td>
<td>Request to Send</td>
<td>Output</td>
</tr>
<tr>
<td>8</td>
<td>CTS+</td>
<td>Clear to Send</td>
<td>Input</td>
</tr>
<tr>
<td>9</td>
<td>CTS-</td>
<td>Clear to Send</td>
<td>Input</td>
</tr>
</tbody>
</table>

Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ts</td>
<td>Storage Temperature, non-operational</td>
<td>-40</td>
<td>85</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>To</td>
<td>Operating Temperature</td>
<td>-34</td>
<td>7</td>
<td>4</td>
<td>C</td>
</tr>
<tr>
<td>Vcc</td>
<td>Power Supply Voltage</td>
<td>4.5</td>
<td>5.5</td>
<td>VDC</td>
<td></td>
</tr>
<tr>
<td>Err</td>
<td>Data Transmission Error Rate</td>
<td>0</td>
<td>.001</td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>
6 Physical and User Interface Details

6.1 User Interface General Description

The User Interface is the device used by a person to operate the ATC. The User Interface of a controller has traditionally consisted of a keyboard and display, and more recently personal computers and personal digital assistants. For example, the User Interface of a NEMA controller is normally a keyboard and display, with NEMA Port 2 allocated to a personal computer or PDA. A 2070 ATC could use a keyboard and display mounted in the door, or a C60P connector allocated to a personal computer or PDA. Going forward, it is the intent of this specification to:

- Preserve compatibility with existing ATC User Interface software
- Create a standard for future advanced User Interfaces, such as graphics
- Adhere to the ATC API specification for software compatibility

It is not the intent of this specification to:

- Preserve User Interface interchangeability among vendors
- Dictate User Interface requirements, other than minimum and optional
- Limit the choices of User Interfaces

6.1.1 Minimum User Interface

The User Interface performs two separate and necessary functions

- User Interface to the Application (Keyboard and Display, for example)
- User Interface to the Shell (Updating application software, operating system and API)

This document requires a minimum interface to the Application, plus a minimum interface to the Shell. This minimum interface provides a common method to enter data and update software for all hardware and software suppliers. In addition to the specified minimum interface, optional interfaces are allowed. User interfaces not specified here as minimum or optional are considered non-compliant.

6.1.1.1 Minimum User Interface to the Application

The minimum user interface to the Application shall consist of the following:
6.1.1.2 Minimum User Interface to the Shell

The minimum User Interface to the Shell shall consist of the following:

- EIA-232 SP4 connector for Shell, 9 pin “D” (Guidance: C50S of 2070 ATC)
- CPU ACTIVE LED Indicator
- Ethernet Port (Guidance: Internal ATC 10/100 hub Port 2)
- USB Port, used only as a memory device

6.1.2 Optional User Interfaces

In addition to the minimum User Interface, the ATC may include one or more optional User Interfaces.

6.1.2.1 Optional User Interfaces to the Application

Option 1: Keyboard, LCD and Bell (Guidance: traditional 2070 ATC)
Option 2: Infrared Port for PDA or Laptop (Guidance: PDA IRDA COM2)
Option 3: Ethernet interface to graphics device (Guidance: Flat panel LCD)

6.1.2.2 Optional User Interfaces to the Shell

Option 1: Infrared Port for PDA or Laptop (Guidance: PDA IRDA COM2)

Guidance:

1. SP4 could possibly do “double duty” for both the Application and Shell. For example, the operating system could use SP4 at power up for downloading new application code. The application could also use SP4 as a front panel interface, with the advantage of freeing one serial port for other uses (SP6). However, if this is applied to an Engine Board is plugged into a 2070 ATC, the front panel data will spew out on C50S instead of controlling the Front Panel. The Application must therefore use the Request Module Status command of the Field I/O determine that the hardware platform is a 2070 ATC requiring the Front Panel data to be redirected to SP6.

2. Ethernet Port 2 is an uplink for a “straight through” cable to a computer, intended to connect a laptop or PDA for diagnostics or software updates.
3. Infrared is specified in the “Communications Interfaces” section, compatible with laptop computers and PDAs. Infrared is simply an alternate media to EIA-232, communicating on the same serial port using light instead of cable.

4. More advanced User Interfaces, such as flat panel LCD or other graphics device may be connected via Ethernet. Hub port 4 is intended for this.

5. The USB port is to be used for memory devices, only as described in the Engine Board section. Networking is implemented via Ethernet, not via USB.

6.1.3 User Interface Pin Connections

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C50 enabled</td>
<td>1</td>
<td>+5VDC</td>
</tr>
<tr>
<td>2</td>
<td>SP4 RXD</td>
<td>2</td>
<td>SP6 RXD</td>
</tr>
<tr>
<td>3</td>
<td>SP4 TXD</td>
<td>3</td>
<td>SP6 TXD</td>
</tr>
<tr>
<td>4</td>
<td>NA</td>
<td>4</td>
<td>NA</td>
</tr>
<tr>
<td>5</td>
<td>DCGND1</td>
<td>5</td>
<td>DCGND1</td>
</tr>
<tr>
<td>6</td>
<td>NA</td>
<td>6</td>
<td>NA</td>
</tr>
<tr>
<td>7</td>
<td>NA</td>
<td>7</td>
<td>CPURESET</td>
</tr>
<tr>
<td>8</td>
<td>NA</td>
<td>8</td>
<td>NA</td>
</tr>
<tr>
<td>9</td>
<td>NA</td>
<td>9</td>
<td>CPULED</td>
</tr>
</tbody>
</table>

Guidance:
The 2070ATC C50 Enabled and C60 Enabled signals have been removed. The functions of C50S and C60S may be replicated simultaneously on other connectors by simply transmitting the SP4 or SP6 on all connectors and logically “ORing” the received data from all connectors into SP4 or SP6.

6.1.4 User Interface Operation

6.1.4.1 Keyboard, LCD and Bell Operation

6.1.4.1.1 Keyboard

The Keyboard, at a minimum, shall be capable of the complete single keystroke functionality (without key translations) of the standard ATC 2070 front panel. Each key shall be engraved or embossed with its function character. Key size and spacing shall equal or exceed that of the 2070 ATC, but the actual keypad arrangement is not specified here.
6.1.4.1.2  **CPU Active LED Indicator**

The cathode of the CPU Active LED Indicator shall be electrically connected to the CPU Activity LED signal and shall have the pull up resistor on the front panel.

6.1.4.1.3  **Display**

The Display shall consist of a Liquid Crystal Display (LCD), a backlight and a contrast control. The contrast control can either be a potentiometer or a software controlled contrast adjustment. If using a potentiometer contrast control, the contrast shall increase with clockwise rotation. If using a software controlled contrast, the contrast control shall be accomplished by pressing the (*) key to enable the adjustment, followed by the (+) key to darken and the (-) key to lighten the contrast. By pressing the (*) key again will disable the contrast adjustment. The contrast adjustment shall provide the entire contrast range of the LCD.

The Display shall have an LED or EL backlight. The backlight shall be turned on and off by the Controller Circuitry. The backlight and associated circuitry shall consume no power when in off state. The Display shall have at a minimum 8 lines of 40 characters each with minimum dimensions of 2.65 mm wide by 4.24 mm high. The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

6.1.4.1.4  **Cursor**

Cursor display shall be turned ON and OFF by command.

- When ON, the cursor shall be displayed at the current cursor position.
- When OFF, no cursor shall be displayed.

All other cursor functions shall remain in effect.

6.1.4.1.5  **Reset**

The User Interface shall be reset once power is applied or have a momentary control reset switch on the PCB that is logic OR'd with the CPU RESET Line, producing a USER Interface RESET. Upon User Interface reset being active or receipt of a valid Soft Reset display command, the following shall occur:

1. Auto-repeat, blinking, auto-wrap, and auto-scroll shall be set to OFF.
2. Each special character shall be set to ASCII SPC (space).
3. The tab stops shall be set to columns 9, 17, 25, and 33.
4. The backlight timeout value shall be set to 6 (60 seconds).
5. The backlight shall be extinguished.
6. The display shall be cleared (all ASCII SPC).
7. The User Interface shall transmit a power up string through /sp6 to the CPU once power is applied to the User Interface, or the User Interface hardware reset switch is pressed. The string is “ESC [PU”, hex value “1B 5B 50 55”.

6.1.4.1.6 Key Press

When a key press is detected, the appropriate key code shall be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code shall be sent. If a key is depressed while another key is depressed, no additional code shall be sent.

6.1.4.1.7 Auto Repeat

Auto-repeat shall be turned ON and OFF by command. When ON, the key code shall be repeated at a rate of 5 times per second starting when the key has been depressed continuously for 0.5 second, and shall terminate when the key is released or another key is pressed.

6.1.4.1.8 Special Characters

The controller circuitry shall be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination with the standard ASCII characters. Undefined characters shall be ignored. User-composed characters shall be represented in the communication protocol on Page 9-7-12 in the TEES. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the top pixel in a column and the least significant bit shall represent the bottom pixel. A logic ‘1’ shall turn the pixel ON. There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an “f.” If the number of Pn's are more than the number of columns available on the LCD, the extra Pn's shall be ignored. P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.

6.1.4.1.9 Character Overwrite

Character overwrite mode shall be the only display mode supported. A displayable character received shall always overwrite the current cursor position on the Display. The cursor shall automatically move right one character position on the Display after each character write operation. When the rightmost character on a line position 40) has been overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.

6.1.4.1.10 Auto Wrap

Auto-wrap shall be turned ON & OFF by command. When ON, a new line operation shall be performed after writing to position 40. When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.
6.1.4.1.11 Cursor Positioning
Cursor positioning shall be non-destructive. Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.

6.1.4.1.12 Blinking
Blinking characters shall be supported, and shall be turned ON and OFF by command. When ON, all subsequently received displayable characters shall blink at the rate of 1 Hz with a 60% ON / 40% OFF duty cycle. It shall be possible to display both blinking and non-blinking characters simultaneously.

6.1.4.1.13 Tab Stops
Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the current cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.

6.1.4.1.14 Auto Scroll
Auto-scroll shall be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one line. When OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.

6.1.4.1.15 Displayable Characters
Displayable characters shall be refreshed at least 20 times per second.

6.1.4.1.16 Backlight Timeout
The Display back light shall illuminate when any key is pressed and shall illuminate or extinguish by command. The backlight shall extinguish when no key is pressed for a specified time. This time shall be program selected by command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals. A value of 1 shall correspond to a timeout interval of 10 seconds. A value of 0 shall indicate no timeout.

6.1.4.1.17 Command Codes
The Command Codes shall use the following conventions:

Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter ‘P’ followed by a lower-case character or number. These are interpreted as follows:
1. **Pn**: Value parameter, to be replaced by a value, using one ASCII character per digit without leading zeros.

2. **P1**: Ordered and numbered parameter. One of a listed known parameters with a specified order and number (Continues with P2, P3, etc.)

3. **Px**: Display column number (1-40), using one ASCII character per digit without leading zero.

4. **Py**: Display line (1-4) one ASCII character ...: Continue the list in the same fashion

   Values of 'h' ($68) and 'l' ($6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).

2. **ASCII Representation**: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.

3. **Hexadecimal Representation**: Characters are shown as their hexadecimal values and will be in the range 00 to 7F (7 bits).

### 6.1.4.18 Communications

The Controller Circuit shall communicate via a SP6 asynchronous serial interface. The interface shall be configured for 38.4 Kbps, 8 data bits, 1 stop bit, and no parity.

### 6.1.4.19 Bell

The User Interface shall include an electronic bell to signal receipt of ^G (hex 07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.

<table>
<thead>
<tr>
<th>ASCII REPRESENTATION</th>
<th>HEX VALUE</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>HT</td>
<td>09</td>
<td>Move cursor to next tab stop</td>
</tr>
<tr>
<td>CR</td>
<td>0D</td>
<td>Position cursor at first position on current line</td>
</tr>
<tr>
<td>LF</td>
<td>0A</td>
<td>(Line Fee) Move cursor down one line</td>
</tr>
<tr>
<td>BS</td>
<td>08</td>
<td>(Backspace) Move cursor one position to the left and write space</td>
</tr>
<tr>
<td>ESC 0 Py j Px f</td>
<td>1B 38 Py 3B Px 66</td>
<td>Position cursor at (Px, Py)</td>
</tr>
<tr>
<td>ESC 0 Pn C</td>
<td>1B 38 Pn 43</td>
<td>Position cursor Pn positions to right</td>
</tr>
<tr>
<td>ESC 0 Pn D</td>
<td>1B 38 Pn 44</td>
<td>Position cursor Pn positions to left</td>
</tr>
<tr>
<td>ESC 0 Pn A</td>
<td>1B 38 Pn 41</td>
<td>Position cursor Pn positions up</td>
</tr>
<tr>
<td>ESC 0 Pn B</td>
<td>1B 38 Pn 42</td>
<td>Position cursor Pn positions down</td>
</tr>
<tr>
<td>ESC 0 H</td>
<td>1B 38 48</td>
<td>Home cursor (move to 1,1)</td>
</tr>
</tbody>
</table>
## CONFIGURATION COMMAND CODES

<table>
<thead>
<tr>
<th>ASCII REPRESENTATION</th>
<th>HEX VALUE</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESC 0 2 J</td>
<td>1B 5B 32 4A</td>
<td>Clear screen with spaces without moving cursor</td>
</tr>
<tr>
<td>ESC c</td>
<td>1B 63</td>
<td>Soft reset</td>
</tr>
<tr>
<td>ESC 0 P1 [ Pn j Pn…f</td>
<td>1B 50 P1 5B Pn 3B…Pn 66</td>
<td>Compose special character number Pn (1-8) at current cursor position</td>
</tr>
<tr>
<td>ESC 0 &lt; Pn V</td>
<td>1B 5B 3C Pn 56</td>
<td>Display special character number Pn (1-8) at current cursor position</td>
</tr>
<tr>
<td>ESC 0 25 h</td>
<td>1B 5B 32 35 68</td>
<td>Turn Character blink on</td>
</tr>
<tr>
<td>ESC 0 25 j</td>
<td>1B 5B 32 35 6C</td>
<td>Turn Character blink off</td>
</tr>
<tr>
<td>ESC 0 &lt; 5 h</td>
<td>1B 5B 3C 35 68</td>
<td>Illuminate Backlight</td>
</tr>
<tr>
<td>ESC 0 &lt; 5 l</td>
<td>1B 5B 3C 35 6C</td>
<td>Extinguish Backlight</td>
</tr>
<tr>
<td>ESC 0 33 h</td>
<td>1B 5B 33 33 68</td>
<td>Cursor blink on</td>
</tr>
<tr>
<td>ESC 0 33 l</td>
<td>1B 5B 33 33 6C</td>
<td>Cursor blink off</td>
</tr>
<tr>
<td>ESC 0 27 h</td>
<td>1B 5B 32 37 68</td>
<td>Reverse video on (Note 2)</td>
</tr>
<tr>
<td>ESC 0 27 l</td>
<td>1B 5B 32 37 6C</td>
<td>Reverse video off (Note 2)</td>
</tr>
<tr>
<td>ESC 0 24 h</td>
<td>1B 5B 32 34 68</td>
<td>Underline on (Note 2)</td>
</tr>
<tr>
<td>ESC 0 24 l</td>
<td>1B 5B 32 34 6C</td>
<td>Underline off (Note 2)</td>
</tr>
<tr>
<td>ESC 0 0 m</td>
<td>1B 5B 30 6D</td>
<td>All attributes off</td>
</tr>
<tr>
<td>ESC H</td>
<td>1B 48</td>
<td>Set tab stop at current cursor position</td>
</tr>
<tr>
<td>ESC 0 Pn g</td>
<td>1B 5B Pn 67</td>
<td>Clear tab stop Pn = 0,1,2 at cursor = 3 all ta stops</td>
</tr>
<tr>
<td>ESC 0 ? 7 h</td>
<td>1B 5B 30 37 68</td>
<td>Auto-wrap on</td>
</tr>
<tr>
<td>ESC 0 ? 7 l</td>
<td>1B 5B 30 37 6C</td>
<td>Auto-wrap off</td>
</tr>
<tr>
<td>ESC 0 ? 8 h</td>
<td>1B 5B 30 38 68</td>
<td>Auto-repeat on</td>
</tr>
<tr>
<td>ESC 0 ? 8 l</td>
<td>1B 5B 30 38 6C</td>
<td>Auto-repeat off</td>
</tr>
<tr>
<td>ESC 0 ? 25 h</td>
<td>1B 5B 30 32 35 68</td>
<td>Cursor on</td>
</tr>
<tr>
<td>ESC 0 ? 25 l</td>
<td>1B 5B 30 32 35 6C</td>
<td>Cursor off</td>
</tr>
<tr>
<td>ESC 0 ? 47 h</td>
<td>1B 5B 3C 34 37 68</td>
<td>Auto-scroll on</td>
</tr>
<tr>
<td>ESC 0 ? 47 l</td>
<td>1B 5B 3C 34 37 6C</td>
<td>Auto-scroll off</td>
</tr>
<tr>
<td>ESC 0 &lt; Pn S</td>
<td>1B 5B 3C Pn 53</td>
<td>Set Backlight timeout value to Pn (0-63)</td>
</tr>
<tr>
<td>ESC 0 Pu</td>
<td>1B 5B 50 55</td>
<td>String sent to CPU when EIPA power up</td>
</tr>
</tbody>
</table>

**NOTE:**

1. Numerical values have one ASCII character per digit without leading zero.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A.
   Reverse Video is NOT required for Option 3B. Command codes shall be available for Option 3C (C60).
INQUIRY COMMAND – RESPONSE CODES

<table>
<thead>
<tr>
<th>COMMAND</th>
<th>RESPONSE</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Module to Front Panel Module</td>
<td>Front Panel Module to CPU Module</td>
<td></td>
</tr>
<tr>
<td>ASCII Representation</td>
<td>HEX Value</td>
<td>ASCII Representation</td>
</tr>
<tr>
<td>ESC 0 6 n</td>
<td>1B 5B 36 60</td>
<td>ESC O Py; Px R</td>
</tr>
<tr>
<td>ESC 0 B n</td>
<td>1B 5B 42 60</td>
<td>ESC O P1; P2;….P6 R</td>
</tr>
<tr>
<td>ESC 0 A n</td>
<td>1B 5B 41 6E</td>
<td>ESC O P1 R</td>
</tr>
</tbody>
</table>

Table 6-1: Configuration Command Codes

6.1.4.2 EIA-232 Port
The above key codes, configuration command codes and inquiry command-response codes may be conveyed via EIA-232 at the same data rates. In lieu of the keyboard and display, an intelligent device, such as a PDA may be used.

6.1.4.3 Infrared Port
This option specifies short distance wireless communications via a modulated light beam. Please refer to the IRDA standards for operation.

6.1.4.4 Ethernet Port
A 10/100 Ethernet port is used for hardwired communications to external devices. Please refer to the IEEE 802.3 standard for operation.

6.1.4.5 USB Port
USB is used as an interface to memory devices. Refer to USB specification.

6.1.4.6 Data Key
Datakey Keyceptacle™ (KC4210, KC4210CB or equal) (optional)
6.1.5 User Interface Power Requirements

The User Interface shall be powered by 4.8 to 5.2 VDC. Any additional voltages required by the User Interface, such as backlight and communications, shall be derived from this single power source. The typical and maximum current requirements of each User Interface shall be published for each device.

6.2 Power Supply General Description

The Power Supply shall be an independent module, cooled by convection only. The Power Supply shall be capable of supporting the internal ATC circuitry, plus provide power for each optional module. The Power Supply shall convert 120 VAC at 60 Hz to the proper DC Voltages at the power rating needed to support the unit and any external power as described in Paragraph 2.6.

6.2.1 "ON/OFF" Power Switch

An "On/Off" POWER Switch shall be provided to disconnect AC from the Power Supply. The “Power On” shall be in the up position.

6.2.2 LED DC Power Indicators

Four LED DC Power Indicators shall be provided to indicate that all required DC voltages meet the following conditions:

a. +5 VDC is within +/-5% and the +/- 12 VDC is within +/-8% of their nominal levels.

b. 332 Parallel I/O versions, the +12 VDC isolated shall be within +/-8%.

c. NEMA versions, the +24 VDC shall be above 21.6 VDC.

6.2.3 Service Voltage Fuse

A replaceable 3AG slow blow fuse shall be provided. Fuse label shall indicate rating.

6.2.4 2.4 +5 VDC Standby Power

+5 VDC Standby Power shall be provided to hold up specified circuitry during the power down period. It shall consist of the monitor circuitry, hold up capacitors, and charging circuitry. A charging circuit shall be provided, that under normal operation, shall fully
charge and float the capacitors consistent with the manufacturers’ recommendations.

The Hold Up power requirements shall be a minimum constant drain of 600 uA at a
range of +5 to +2 VDC for over 600 minutes. Capacitors shall be fully charged within 10
minutes.

6.2.5 Monitor Circuitry

Monitor Circuitry shall be provided to monitor incoming Service Power for Power failure
and Restoration and LINESYNC generation.

6.2.5.1 Service Fail/Power Down and Sysreset/Power Up

Power Fail Calibration for CALTRANS Cabinets:

The Service FAIL/POWER DOWN Output Lines shall go LOW (ground true) immediately
when the service voltage falls below 92 +/-2 VAC. The Lines shall transition to HIGH
when the service voltage exceeds 97 +/- 2 VAC. The Lines shall be driven separately.

Power Fail Calibration for NEMA Cabinets:

The Service FAIL/POWER DOWN Output Lines shall go LOW (ground true) immediately
when the service voltage falls below 85 +/-2 VAC. The Lines shall transition to HIGH
when the service voltage exceeds 90 +/- 2 VAC. The Lines shall be driven separately.

The SYSRESET/POWERUP Output Lines shall transition to LOW 525 +/- 25 ms after
Service FAIL/POWER DOWN transition to LOW. The Lines shall transition to HIGH 225
+/- 25 ms after Power Restoration and the supply is fully recovered. The Lines shall be
driven separately.

6.2.5.2 Linesync

The 60 Hz Square Wave LINESYNC signal shall be generated by a crystal oscillator,
which shall synchronize to the 60-Hz service power line at 120 and 300 degrees. A
continuous square wave signal shall be +5 VDC amplitude, 8.333 ms half-cycle pulse
duration, and 50 +/- 1% duty cycle. The output shall have drive sink capability of 16 mA.
The monitor circuit shall compensate for missing pulses and line noise during normal
operation. The LINESYNC shall continue operating after power fail until loss of 5 VDC
regulation. LINESYNC crystal oscillator shall have an accuracy of +/- 0.005% at 25 C.

6.2.6 External Power Supply Requirements

The following external voltages shall be within these parameters.

Each Optional Communications Interface Module:
6.2.6.1 Line and Load Regulation

The Power Supply shall meet the external voltage tolerances for minimum and maximum loads called out.

  a. 332 Parallel I/O Version: 100 VAC to 135 VAC +/- 2 VAC
  b. NEMA: 89 VAC to 135 VAC +/- 2 VAC

6.2.6.2 Ripple and Noise

Less than 0.5% rms, 2% peak to peak, whichever is greater.

6.2.6.3 Over Voltage

The Power Supply shall clamp at 130% Vout for all outputs.

6.2.6.4 Inrush Current

Cold Start Inrush shall be less than 25A at 115VAC.

6.2.6.5 Holdup Time

The power supply shall supply +5VDC current budget for 550 ms after power loss at 100 VAC. The supply shall be capable of holding up the ATC for two 500 ms Power Loss periods occurring in a 1.5-second period at 100 VAC. Since the Engine Board is powered completely by +5 VDC, no other power supply output voltages shall need to be maintained during power loss to prevent reboot.
6.3 Mechanical and Physical General Description

The ATC Mechanical and Physical attributes provide mechanical enclosure and human engineering, including:

- Maximum Size
- Form Factor
- Mounting and Installation Method
- Materials
- Structural Integrity
- Ease of Use
- Cost Effectiveness

It is the intent of this specification to:

- Preserve compatibility with existing cabinet styles
- Reduce the size and complexity of existing controllers
- Improve human engineering for intuitive use of complex control functions

It is not the intent of this specification to:

- Interchange electronic modules and mechanical assemblies among vendors (except Communications Interface and Engine Board)
- Dictate mechanical details
- Preserve existing controller sizes and form factors

6.3.1 Chassis

6.3.1.1 Construction Materials
The CHASSIS including supports, mounting surfaces, power supply enclosures and front panel shall be made of 0.063-inch minimum aluminum sheet metal or equivalent strength non-corrosive material. Construction materials shall withstand all environmental standards of this specification.

6.3.1.2 Weight
The total composition weight shall not exceed 25 pounds.
6.3.1.3 Mounting Method

As a minimum, the chassis shall be capable of mounting to a Standard EIA 310-B Rack using 4U (or smaller standard increment) open end mounting slots. If not rack mounted, EIA 310-B does not apply and other chassis mounting methods are allowed, not to exceed overall dimensions specified here. Mounting method shall withstand all mechanical shock and vibration requirements of this standard.

6.3.1.4 Dimensions (All dimensions are given in inches)

Details of Maximum Basic Dimensions (not restricted to shape shown)

![Figure 6-1: Maximum Basic Dimensions](image)

**Guidance:**

These maximum dimensions were chosen for the following reasons:

1. NEMA TS-1 2070ATC users requested dimensions smaller than the 2070N to compensate for equipment added to NEMA cabinets, such as video.
2. The size chosen is the only size meeting all of the following specifications:
   - NEMA TS-2, Shelf Mount (NEMA TS-2, Paragraph 3.2.1)
   - NEMA TS-2, Rack Mount (NEMA TS-2, Paragraph 3.2.1)
   - 2070ATC, Rack Mount for 332 Cabinets (2070-2A Field I/O)
   - 2070ATC, Rack Mount for ITS Cabinets (2070-2B Field I/O)
   - 2070ATC, Shelf Mount for TS-2 Type 1 NEMA Cabinets (2070-2N Field I/O)
Quoting NEMA TS-2 Specification, Paragraph 3.2.1 Dimensions:

“The CU shall be capable of being shelf mounted. The CU shall also be capable of being mounted in a 19-inch rack (EIA Standard RS-310-C, 1982). The height of the CU shall not exceed 30.48 cm (12 in.). The depth of the unit, including connectors, harnesses, and protrusions, shall not exceed 36.83 cm (14.5 in.). On rack-mounted units, the mounting flanges of the control unit shall be so placed that no protrusion shall exceed 27.94 cm (11 in.) to the rear and 8.89 cm (3.5 in.) to the front.”

Note A –

Minimum and Optional components located on front of assembly are as follows:

- C50S - 9-Pin DB Socket Type
- C60P - 9-Pin DB Plug Type
- Infrared Communication Port
- Front Panel Display
- Keyboard
- ON/OFF Power Switch
- Power Supply Service Fuse Holder (with 3AG fuse)
- LED for each DC power source and “ACTIVE” indications
- USB series A 4 Pin Receptacle Communication Port
- RJ-45 Connector ETHERNET Port Uplink Hub Port
- Two Ethernet LEDs, labeled “100” and “ACTIVE”
- Datakey Keyceptacle™ KC4210, KC4210CB or equal

Note B –

Minimum and Optional components located on rear of assembly (rack mount) or on the front of assembly (shelf mount) are as follows:

- Parallel I/O C1S - M104 Type
- C11S – 37-Pin Circular Plastic Type
- Serial I/O C12S – 25-Pin DB Socket Type
- C13S – 25-Pin DB Socket Type
- ATC Communications Interface Slots, One or More
- RJ-45 Connector ETHERNET Network Hub Port
- Two Ethernet LEDs, labeled “100” and “ACTIVE”
- Transmitter and Receiver activity is displayed on the “ACTIVITY” LED. The “100” LED is illuminated when the hub port is linked at 100 Mbps and extinguished at all other times. LEDs shall employ clear lenses.
7 Parallel and Serial I/O Details

7.1 General Information

The ATC Input / Output (I/O) provides both serial and parallel connections to field devices connected to the ATC, as well as the input of service power.

7.1.1 Parallel Input / Output Overview

The parallel I/O connects the ATC to transportation cabinets including, but not limited to, the following:

- NEMA TS-1
- NEMA TS-2 Type 1
- NEMA TS-2 Type 2
- CALTRANS 332
- Joint NEMA/AASHTO/ITE/CALTRANS Intelligent Transportation System

Note that this parallel I/O specification does not include Versa Module Europe (VME) or any other parallel high-speed computer bus. Access to devices residing on a high-speed computer bus shall be interfaced via the ATC Ethernet hub port 4. The user is responsible for providing an external rack, power supply, high-speed bus and Ethernet interface module residing in this external rack, as well as all Ethernet software drivers.

7.1.2 Serial I/O Overview

The serial connections described here provides communications for implementation of existing transportation standards, including but not limited to, the following:

- NEMA TS-2
- NEMA TS-2 Type 1
- NEMA TS-2 Type 2
- CALTRANS Type 170
- Joint NEMA/AASHTO/ITE/CALTRANS 2070 ATC
7.1.3 Power Input Overview

The power input provides a service power connection per existing transportation standards, including but not limited to, the following:

- NEMA TS-2
- NEMA TS-2 Type 1
- NEMA TS-2 Type 2
- CALTRANS Type 170
- Joint NEMA/AASHTO/ITE/CALTRANS 2070 ATC

7.2 Parallel Input / Output (PI/O)

7.2.1 Parallel Connection to CALTRANS 332 Style Cabinets

The parallel connection to a CALTRANS 332 Style Cabinet shall consist of the Field Controller Unit, Parallel Input/Output Ports, Connectors C1S, and C11S, and other Module Circuit Functions including muzzle jumper.

7.2.1.1 Field Controller Unit (FCU)

The FCU shall include a programmable microprocessor/controller unit together with all required clocking and support circuitry. Operational software necessary to meet housekeeping and functional requirements shall be provided resident in socketed firmware or FLASH.

7.2.1.2 Parallel I/O Ports

The I/O Ports shall provide 64 bits of input using ground-true logic. Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 µA or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to the isolated +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground.
7.2.1.2.1 Parallel I/O Port Electrical

The I/O Ports shall provide 64 bits of output. Each output written as a logic "1" shall have a voltage at its field connector output of less than 4.0 VDC. Each output written as logic "0" shall provide an open circuit (1 megohm or more) at its field connector output. Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 mA minimum. Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 µs when connected to a load of 100 K-Ohms minimum. Each output circuit shall be protected from transients of 10 ±2 µs duration, ±300 VDC from a 1 K-Ohm source, with a maximum rate of 1 pulse per second.

7.2.1.2.2 Parallel I/O Port Timing

Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing. The state of all output circuits at the time of Power Up or in Power Down state shall be open. It shall be possible to simultaneously assert all outputs within 100 µs of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

7.2.1.3 Other Parallel I/O Functions

7.2.1.3.1 Signals and Capacitive Load

A maximum capacitive load of 100 pF shall be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.

7.2.1.3.2 Legacy Signal Monitors

An External WDT "Muzzle" Jumper shall be provided internal to the ATC. With the jumper IN and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output Port 5, bit 8 (Connector C1, pin 103 – Monitor Watchdog Timer Input) every 100 ms for 10 seconds or due to CPU Command. When the jumper is missing, the feature shall not apply.

This feature is required to operate with the Model 210 Monitor Unit only. The Model 210 Monitor requires activity on pin 103 immediately after power-up to determine that the ATC is functioning. Without the Muzzle Jumper installed, the ATC boot-up time prevents the application software from performing this task in time. If the controller is truly malfunctioning, the activity on pin 103 ceases within 10 seconds.

More modern Monitors have an adjustable power up time, allowing the intersection to remain in FLASH until the controller has booted-up and the application software begins to toggle pin 103.
7.2.1.3.3 **Watchdog Circuit**

A WATCHDOG Circuit shall be provided. It shall be enabled by the software at Power Up with a value of 100ms. Its enabled state shall be machine readable and reported in the status byte. Once enabled, the watchdog timer shall not be disabled without resetting the PI/O. Failure of the PI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.

7.2.1.3.4 **One KHz Reference**

A synchronizable 1 KHz time reference shall be provided. It shall maintain a frequency accuracy of ±0.01% (±0.1 counts per second).

7.2.1.3.5 **Millisecond Counter**

A 32-bit Millisecond Counter (MC) shall be provided for “time stamping.” Each 1 KHz reference interrupt shall increment the MC.

7.2.1.3.6 **Communications Loss**

At Power Up, the FCU loss of communications timer shall indicate loss of communications with the ATC until the user program sends the Request Module Status message to reset the “E” Bit and a subsequent set output command is processed.

7.2.1.3.7 **Control Signals**

LINESYNC and POWER DOWN Lines shall be isolated and routed to FCU for shut down functions. CPU RESET and POWER UP (SYSRESET) Lines shall be isolated and logically “OR’d” to form NRESET. NRESET shall be used to reset FCU and other module devices.

7.2.1.3.8 **Isolation**

Isolation shall be provided between internal +5DC / DCG#1 and +12 DC ISO/DCG#2. +12 DC ISO shall be used for board power and external logic.

7.2.1.4 **Buffers**

A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries. The Transition Buffer shall default to empty. There shall be two entry types: Transition and Rollover. The inputs shall be monitored for state transition. At each transition (If the input has been configured to report transition), a transition entry shall be added to the Transition Buffer. The MC shall be monitored for rollover. At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry shall be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the CPU module upon command.
Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer. The entry types are depicted as follows:

### Input Transition Entry

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transition Entry Identifier</td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Timestamp NLSB</td>
<td>x</td>
<td>x x x x x</td>
<td>2</td>
</tr>
<tr>
<td>Timestamp LSB</td>
<td>x</td>
<td>x x x x x</td>
<td>3</td>
</tr>
</tbody>
</table>

### Millisecond Counter Rollover Entry

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rollover Entry Identifier</td>
<td>1</td>
<td>1 1 1 1 1</td>
<td>1</td>
</tr>
<tr>
<td>Timestamp MSB</td>
<td>x</td>
<td>x x x x</td>
<td>2</td>
</tr>
<tr>
<td>Timestamp NMSB</td>
<td>x</td>
<td>x x x x</td>
<td>3</td>
</tr>
</tbody>
</table>

#### 7.2.1.5 I/O Functions

##### 7.2.1.5.1 Inputs

**Input Scanning**

Input scanning shall begin at I0 (bit 0) and proceed to the highest input, ascending from Isb to msb. Each complete input scan shall finish within 100 µs. Once sampled, the Logic State of input shall be held until the next input scan. Each input shall be sampled 1,000 times per second. The time interval between samples shall be 1 ms ±100 µs. If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer. If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing number. The MC shall be sampled within 10 µs of the completion of the input scan.

**Data Filtering**

If configured, the inputs shall be filtered by the FCU to remove signal bounce. The filtered input signals shall then be monitored for changes as noted. The filtering parameters for each input shall consist of Ignore Input Flag and the On and Off filter samples. If the Ignore Input flag is set, no input transitions shall be recorded. The On and Off filter samples shall determine the number of consecutive samples an input must be on and off, respectively, before a change of state is recognized. If the change of state is shorter than the specified value, the change of state shall be ignored. The On and Off filter values shall be in the range of 0 to 255. A filter value of 0, for either or both values, shall result in no filtering for this input. The default values for input signals after reset shall be as follows:
Filtering Enabled
On and off filter values set to 5
Transition monitoring Disabled (Timestamps are not logged)

7.2.1.5.2 Outputs
Simultaneous assertion of all outputs shall occur within 100 µs. Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC. The condition of the outputs shall only be "ON" if the PI/O continues to receive active communications from the CPU Module. If there is no valid communications with the CPU Module for 2.0 seconds, all outputs shall revert to the OFF condition, and the PI/O status byte shall be updated to reflect the loss of communication from the CPU Module.

Standard Function
Each output shall be controlled by the data and control bits in the CPU Module-PI/O frame protocol as follows:

<table>
<thead>
<tr>
<th>Case</th>
<th>Output Data Bit</th>
<th>Output Control Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0</td>
<td>0</td>
<td>Output in the OFF state</td>
</tr>
<tr>
<td>B</td>
<td>1</td>
<td>1</td>
<td>Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.</td>
</tr>
<tr>
<td>C</td>
<td>0</td>
<td>1</td>
<td>Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF</td>
</tr>
<tr>
<td>D</td>
<td>1</td>
<td>0</td>
<td>Output is in the ON state.</td>
</tr>
</tbody>
</table>

Output Stability
In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured. For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 µs after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle. In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON remain ON until otherwise configured. All outputs shall not glitch nor change state unless configured to do so.

7.2.1.6 Other Processor Functions

7.2.1.6.1 Interrupts
All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts. MILLISECOND Interrupt shall be activated by the 1 KHz
reference once per ms. A timestamp rollover flag set by MC rollover shall be cleared only on command. LINESYNC interrupt - This interrupt shall be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal. The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds (≥60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer (≥500 consecutive millisecond interrupts).

7.2.1.6.2 Communication Service Routine
A low-level communication service routine shall be provided to handle reception, transmission, and communication faults.

7.2.1.6.3 Communication Processing
The task shall be to process the command messages received from the CPU Module, prepare, and start response transmission. The response message transmission shall begin within 4 ms of the receipt of the received message. Message type processing time constraints shall not exceed 70 ms per message.

7.2.1.6.4 Input Processing
This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

7.2.1.7 Data Communications Protocols

7.2.1.7.1 Protocols
All communication with the CPU Module shall be via command-response protocol. The CPU Module shall always initiate the communication and should the command frame be incomplete or in error, no PI/O response shall be transmitted. The amount of bytes of a command or response is dependent upon the I/O Module identification. The physical interface is not controlled by this specification, and interchangeability among vendors from PI/O to Engine Board is not intended. For example, communications to PI/O module may be implemented via EIA-485 at 614 K bps, 5V TTL, or via a 1 GHz fiber channel, provided all PI/O specifications herein are met, including:

- Command and Response Message Content
- Command and Response Timing
- Error Checking
- Electrical Isolation
Therefore, a “frame” is merely a field in the data stream, not related to the physical interface between the CPU and the PI/O.

7.2.1.7.1.1 Frame Types

The frame type shall be determined by the value of the first byte of the message. The command frames type values $70 - $7F and associated response frame type values $F0 - $FF are allocated to the Contractor diagnostics. All other frame types not called out are reserved. The command-response Frame Type values and message times shall be as follows:

**Guidance:**

The following Commands and Responses are intended to match the CALTRANS TEES and the Joint NEMA/AASHTO/ITE 2070 ATC commands and responses.

<table>
<thead>
<tr>
<th>Module Command</th>
<th>I/O Module Response</th>
<th>Description</th>
<th>Minimum Message Time</th>
<th>Maximum Message Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>49</td>
<td>177</td>
<td>Request Module Status</td>
<td>250 µs</td>
<td>275 us</td>
</tr>
<tr>
<td>50</td>
<td>178</td>
<td>MILLISECOND CTR. Mgmt.</td>
<td>222.5 µs</td>
<td>237.5 us</td>
</tr>
<tr>
<td>51</td>
<td>179</td>
<td>Configure Inputs</td>
<td>344.5 µs</td>
<td>6.8750 ms</td>
</tr>
<tr>
<td>52</td>
<td>180</td>
<td>Poll Raw Input Data</td>
<td>317.5 µs</td>
<td>320 µs</td>
</tr>
<tr>
<td>53</td>
<td>181</td>
<td>Poll Filtered Input Data</td>
<td>317.5 µs</td>
<td>320 µs</td>
</tr>
<tr>
<td>54</td>
<td>182</td>
<td>Poll Input Transition Buffer</td>
<td>300 µs</td>
<td>10.25 ms</td>
</tr>
<tr>
<td>55</td>
<td>183</td>
<td>Command Outputs</td>
<td>405 µs</td>
<td>410 µs</td>
</tr>
<tr>
<td>56</td>
<td>184</td>
<td>Config. Input Tracking Functions</td>
<td>340 µs</td>
<td>10.25 ms</td>
</tr>
<tr>
<td>57</td>
<td>185</td>
<td>Config. Complex Output Functions</td>
<td>340 µs</td>
<td>6.8750 ms</td>
</tr>
<tr>
<td>58</td>
<td>186</td>
<td>Configure Watchdog</td>
<td>222.5 µs</td>
<td>222.5 µs</td>
</tr>
<tr>
<td>59</td>
<td>187</td>
<td>Controller Identification</td>
<td>222.5 µs</td>
<td>222.5 µs</td>
</tr>
<tr>
<td>60</td>
<td>188</td>
<td>I/O Module Identification</td>
<td>222.5 µs</td>
<td>222.5 µs</td>
</tr>
<tr>
<td>61-62-65</td>
<td>189-190-193</td>
<td>Reserved (note below)</td>
<td>317.5 us</td>
<td>320 us</td>
</tr>
<tr>
<td>64</td>
<td>191-192</td>
<td>Poll variable length raw input</td>
<td>405 us</td>
<td>410 us</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Variable length command outputs</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

7.2.1.7.1.2 ITS Cabinet Frames

Messages 61 / 189, 62 / 190 and 65 / 193 are for ITS Cabinet Monitor Unit. See ITS Cabinet Monitor System Serial Bus #1 for Command and Response Frames. Message 63 / Message 191 shall be the same as Message 52 / 180 except Byte 2 of Message 180 response shall denote the following number of input bytes. Message 64 / 192 shall be the same as Message 55 / 183 except Byte 2 of the Message 55 Command shall denote the number of output data bytes plus the following output data.
7.2.1.7.2 Request Module Status

The Command shall be used to request PI/O status information response. Command/response frames are as follows:

<table>
<thead>
<tr>
<th>Description</th>
<th>Msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 49)</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Reset Status Bits</td>
<td>P</td>
<td>E</td>
<td>K</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>T</td>
<td>M</td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>W</td>
<td></td>
</tr>
</tbody>
</table>

Request Module Status Command

<table>
<thead>
<tr>
<th>Description</th>
<th>Msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 177)</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>System Status</td>
<td>P</td>
<td>E</td>
<td>K</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>T</td>
<td>M</td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>W</td>
<td></td>
</tr>
<tr>
<td>SCC Receive Error Count</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCC Transmit Error Count</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timestamp MSB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timestamp NMSB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timestamp NLSB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timestamp LSB</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Request Module Status Response

<table>
<thead>
<tr>
<th>Description</th>
<th>Msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 177)</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>System Status</td>
<td>P</td>
<td>E</td>
<td>K</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>T</td>
<td>M</td>
</tr>
<tr>
<td></td>
<td>L</td>
<td>W</td>
<td></td>
</tr>
</tbody>
</table>

7.2.1.7.2.1 Request Module Status Response

The response status bits are defined as follows:

P - Indicates PI/O hardware reset
E - Indicates a communications loss of greater than 2 seconds
M - Indicates an error with the MC interrupt
L - Indicates an error in the LINESYNC
W - Indicates that the PI/O has been reset by the Watchdog
R - Indicates that the EIA-485 receive error count byte has rolled over
T - Indicates that the EIA-485 transmit error count byte has rolled over
K - Indicates the Datakey has failed or is not present

7.2.1.7.2.2 Bit Information

Each of these bits shall be individually reset by a ‘1’ in the corresponding bit of any subsequent Request Module Status frame, and the response frame shall report the current status bits. The SCC error count bytes shall not be reset. When a count rolls over (255 - 0), its corresponding roll-over flag shall be set.
7.2.1.7.3 MC Management Frame

MC management frame shall be used to set the value of the MC. The ‘S’ bit shall return status ‘0’ on completion or ‘1’ on error. The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

<table>
<thead>
<tr>
<th>Description</th>
<th>Msb</th>
<th>Lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 50)</td>
<td>0 0 1 1 0 0 1 0</td>
<td>Byte 1</td>
<td></td>
</tr>
<tr>
<td>New Timestamp MSB</td>
<td>X x x x x x x x</td>
<td>Byte 2</td>
<td></td>
</tr>
<tr>
<td>New Timestamp NMSB</td>
<td>X x x x x x x x</td>
<td>Byte 3</td>
<td></td>
</tr>
<tr>
<td>New Timestamp NLSB</td>
<td>X x x x x x x x</td>
<td>Byte 4</td>
<td></td>
</tr>
<tr>
<td>New Timestamp LSB</td>
<td>X x x x x x x x</td>
<td>Byte 5</td>
<td></td>
</tr>
</tbody>
</table>

7.2.1.7.4 Configure Inputs

The Configure Inputs command frame shall be used to change input configurations. The command-response frames are as follows:

<table>
<thead>
<tr>
<th>Description</th>
<th>Msb</th>
<th>Lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 51)</td>
<td>0 0 1 1 0 0 1 1</td>
<td>Byte 1</td>
<td></td>
</tr>
<tr>
<td>Number of Items (n)</td>
<td>n n n n n n n n</td>
<td>Byte 2</td>
<td></td>
</tr>
<tr>
<td>Item # - Byte 1</td>
<td>E Input Number</td>
<td>Byte 3(I-1)+3</td>
<td></td>
</tr>
<tr>
<td>Item # - Byte 2</td>
<td>Leading edge filter (e)</td>
<td>Byte 3(I-1)+4</td>
<td></td>
</tr>
<tr>
<td>Item # - Byte 3</td>
<td>Trailing edge filter (r)</td>
<td>Byte 3(I-1)+5</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
<th>Msb</th>
<th>Lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 179)</td>
<td>1 0 1 1 0 0 1 1</td>
<td>Byte 1</td>
<td></td>
</tr>
<tr>
<td>Status</td>
<td>0 0 0 0 0 0 0 S</td>
<td>Byte 2</td>
<td></td>
</tr>
</tbody>
</table>

Block field definitions shall be as follows:

- E - Ignore Input Flag.
- "1" = do not report transitions for this input,
- "0" = report transitions for this input
- e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled)
7.2.1.7.5 **Poll Raw Input Data**

The Poll Raw Input Data frame shall be used to poll the PI/O for the current unfiltered status of all inputs. The response frame shall contain 8 or 15 bytes of information indicating the current input status. The frames are as follows:

<table>
<thead>
<tr>
<th>Poll Raw Input Data Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
</tr>
<tr>
<td>(Type Number = 52)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Poll Raw Input Data Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
</tr>
<tr>
<td>(Type Number = 180)</td>
</tr>
<tr>
<td>Inputs I0 (lsb) to I7 (msb)</td>
</tr>
<tr>
<td>Inputs I8 to I119</td>
</tr>
<tr>
<td>Timestamp MSB</td>
</tr>
<tr>
<td>Timestamp NMSB</td>
</tr>
<tr>
<td>Timestamp NLSB</td>
</tr>
<tr>
<td>Timestamp LSB</td>
</tr>
</tbody>
</table>

7.2.1.7.6 **Poll Input Filtered Data**

The Poll Filtered Input Data frame shall be used to poll the PI/O for the current filtered status of all inputs. The response frame shall contain 8 bytes(-2A) or 15 bytes (2B) of information indicating the current filtered status of the inputs. Raw input data shall be provided in the response for inputs that are not configured for filtering. The frames are as follows:

<table>
<thead>
<tr>
<th>Poll Filter Input Data Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
</tr>
<tr>
<td>(Type Number = 53)</td>
</tr>
</tbody>
</table>
Poll Filter Input Data Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 181)</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Inputs I0 (lsb) to I7 (msb)</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Inputs I8 to I119</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Timestamp MSB</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Timestamp NMSB</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Timestamp NLSB</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Timestamp LSB</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>

### 7.2.1.7.7 Poll Input Transition Buffer

The Poll Input Transition Buffer frame shall poll the PI/O for the contents of the input transition buffer. The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:

Poll Input Transition Buffer Command

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 54)</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Block Number</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>

Input Transition Buffer Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 182)</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Block Number</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Number of Entries</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Item #</td>
<td>S</td>
<td>Input Number</td>
<td>Byte 3(I-1)+4</td>
</tr>
<tr>
<td>Item # Timestamp NLSB</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Item # Timestamp LSB</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Status</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Timestamp MSB</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Timestamp NMSB</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Timestamp NLSB</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Timestamp LSB</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>

### 7.2.1.7.7.1 State Transitions

Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. Bit definitions are as follows:
7.2.1.7.7.2 Block Number
The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module. When the PI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer shall be re-sent to the CPU Module and the 'E' flag set in the status response frame. If it is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent. If the block number is not incremented by one, the status G bit shall be set. The block number received becomes the current number (even if out of sequence). The Block Number byte sent in the response block shall be the same as that received in the command block. Counter rollover shall be considered as a normal increment.

7.2.1.8 Set Outputs
The Set Outputs frame shall be used to command the PI/O to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to '1'. If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set. Loss of LINESYNC reference shall also be indicated in system status information. The output bytes depend upon field I/O module. These command and response frames are as follows:

<table>
<thead>
<tr>
<th>Set Outputs Command</th>
<th>Msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 55)</td>
<td>0</td>
<td>0</td>
<td>1 1 1 1</td>
</tr>
<tr>
<td>Outputs 00 (lsb) to O7 (msb) Data</td>
<td>x x x x x x</td>
<td>Byte 2</td>
<td></td>
</tr>
<tr>
<td>Outputs O8 to O103 Data</td>
<td>x x x x x x x x</td>
<td>Bytes 3 to 14</td>
<td></td>
</tr>
<tr>
<td>Outputs O0 (lsb) to O7 (msb) Control</td>
<td>x x x x x x x</td>
<td>Byte 15</td>
<td></td>
</tr>
<tr>
<td>Outputs O8 to O103 Control</td>
<td>x x x x x</td>
<td>Byte 16 to 27</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Set Outputs Response</th>
<th>Msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 183)</td>
<td>1</td>
<td>0</td>
<td>1 1 1 1</td>
</tr>
<tr>
<td>Status</td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 L E</td>
</tr>
<tr>
<td>Byte 2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

7.2.1.9 Configure Input Tracking Functions
The Configure Input Tracking Functions frame shall be used to configure outputs to respond to transitions on a specified input. Each Output Number identified by Item
Number shall respond as configured to the corresponding Input Number identified by the same Item Number. Input to Output mapping shall be one to one. If a command results in more than 8 input tracking outputs being configured, the response V bit shall be set to ‘1’ and the command shall not be implemented. The command and response frames are as follows:

### Configure Input Tracking Functions Command

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 56)</td>
<td>0</td>
<td>0</td>
<td>0 1 1 1 0 0 0</td>
</tr>
<tr>
<td>Number of Items</td>
<td></td>
<td></td>
<td>Number of Items</td>
</tr>
<tr>
<td>Item # - Byte 1</td>
<td>E</td>
<td></td>
<td>Output Number</td>
</tr>
<tr>
<td>Item # - Byte 2</td>
<td>I</td>
<td></td>
<td>Input Number</td>
</tr>
</tbody>
</table>

### Configure Input Tracking Functions Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 184)</td>
<td>1</td>
<td>0</td>
<td>0 1 1 1 0 0 0 V</td>
</tr>
<tr>
<td>Status</td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 0 0 0 0 V</td>
</tr>
<tr>
<td>Timestamp MSB</td>
<td>x</td>
<td>x</td>
<td>X x x x x x X</td>
</tr>
<tr>
<td>Timestamp NMSB</td>
<td>x</td>
<td>x</td>
<td>X x x x x x X</td>
</tr>
<tr>
<td>Timestamp NLSB</td>
<td>x</td>
<td>x</td>
<td>X x x x x x X</td>
</tr>
<tr>
<td>Timestamp LSB</td>
<td>x</td>
<td>x</td>
<td>X x x x x x X</td>
</tr>
</tbody>
</table>

#### 7.2.1.9.1 Configure Input Tracking Functions Response

Definitions are as follows:

- **E '1'** - Enable input tracking functions for this output
- **'0'** - Disable input tracking functions for this output
- **I '1'** - The output is OFF when input is ON, ON when input OFF
- **'0'** - The output is ON when input is ON, OFF when input is OFF
- **V '1'** - The max. number of 8 configurable outputs exceeded
- **'0'** - No error

Number of Items - The number of entries in the frame. If zero, all outputs currently configured for input tracking shall be disabled.

#### 7.2.1.9.2 Timestamp

The timestamp value shall be sampled prior to the response frame.

#### 7.2.1.9.3 Output Updates

Outputs which track inputs shall be updated no less than once per ms. Input to output signal propagation delay shall not exceed 2 ms.
7.2.1.9.4 Number of Item Field

The “Number of Item” field is valid from 0 to 16 (most that is sent at one time is 8 enables and 8 disables). If processing a command resulting in more than 8 Input Tracking functions being enabled, none of the command shall be implemented and response message “V” bit set to 1. If an invalid output or input number is specified for a function, the FIOM software shall not do that function definition. It shall also not be counted toward the maximum of 8 input tracking function allowed. The rest of the message shall be processed. When an Input Tracking function is disabled, the output is set according to the most recently received Set Outputs Command. When an input tracking function for an output is superseded (redefined as either another input tracking function, or as a complex output function) nothing shall be done with the output. The most recent value remains until the new function changes it.

7.2.1.10 Configure Complex Output Functions

The Configure Complex Output Functions frame shall be used to specify a complex output for one to eight of any of the outputs. If a Configure Complex Output Function command results in more than eight outputs being configured, the 'V' bit in the response message shall be set to a '1', and the command shall not be implemented. Two output forms shall be provided, single pulse and continuous oscillation. These output forms shall be configurable to begin immediately or on a specified input trigger and, in the case of continuous oscillation, to continue until otherwise configured or to oscillate only while gated active by a specified input. If the command gate bit is active, the command trigger bit shall be ignored and the specified input shall be used as a gate signal. The command and response frames are as follows:

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 57)</td>
<td>0 0 1 1</td>
<td>0 0 1</td>
<td>Byte 1</td>
</tr>
<tr>
<td>Number of Items</td>
<td>Number of Items</td>
<td></td>
<td>Byte 2</td>
</tr>
<tr>
<td>Item # - Byte 1</td>
<td>0</td>
<td>Output Number</td>
<td>Byte 7(I-1)+3</td>
</tr>
<tr>
<td>Item # - Byte 2</td>
<td>Primary Duration (MSB)</td>
<td></td>
<td>Byte 7(I-1)+4</td>
</tr>
<tr>
<td>Item # - Byte 3</td>
<td>Primary Duration (LSB)</td>
<td></td>
<td>Byte 7(I-1)+5</td>
</tr>
<tr>
<td>Item # - Byte 4</td>
<td>Secondary Duration (MSB)</td>
<td></td>
<td>Byte 7(I-1)+6</td>
</tr>
<tr>
<td>Item # - Byte 5</td>
<td>Secondary Duration (LSB)</td>
<td></td>
<td>Byte 7(I-1)+7</td>
</tr>
<tr>
<td>Item # - Byte 6</td>
<td>0</td>
<td>Input Number</td>
<td>Byte 7(I-1)+8</td>
</tr>
<tr>
<td>Item # - Byte 7</td>
<td>P W G E J F R L</td>
<td></td>
<td>Byte 7(I-1)+9</td>
</tr>
</tbody>
</table>
Configure Complex Output Functions Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 185)</td>
<td>1</td>
<td>0</td>
<td>1 1 1 0 0 1</td>
</tr>
<tr>
<td>Status</td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 0 0</td>
</tr>
<tr>
<td>Timestamp (MSB)</td>
<td>x</td>
<td>x</td>
<td>x x x x x</td>
</tr>
<tr>
<td>Timestamp (NMSB)</td>
<td>x</td>
<td>x</td>
<td>x x x x x</td>
</tr>
<tr>
<td>Timestamp (NLSB)</td>
<td>x</td>
<td>X</td>
<td>x x x x x</td>
</tr>
<tr>
<td>Timestamp (LSB)</td>
<td>x</td>
<td>X</td>
<td>x x x x x</td>
</tr>
</tbody>
</table>

7.2.10.1 Configure Complex Outputs Bit Fields

The bit fields of the command frame are defined as follows:

- **E '1'** - enable complex output function for this output
- **'0'** - disable complex output function for this output
- **J '1'** - During the primary duration, the output shall be written as a logic '1'.
- **'0'** - During the secondary duration, the output shall be written as a logic '0'.

Output Number - 7-bit output number identifying outputs

Primary Duration - For single pulse operation, this shall determine the number of 'ticks' preceding the pulse. For continuous oscillation, this shall determine the length of the inactive (first) portion of the cycle.

Secondary Duration - For single pulse operation, this shall determine the number of 'ticks' the pulse is active. Subsequent to the secondary duration, the output shall return to the state set according to the most recently received Set Outputs command. For continuous oscillation, this shall determine the length of the active (second) portion of the cycle. 0 = hold output state until otherwise configured.

- **F '1'** - The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.
- **'0'** - The trigger or gate shall be derived from the raw input.

- **R '1'** - For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.
- **'0'** - For triggered output, the output shall be triggered by an OFF-to-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON.
Input Number - 7-bit input number identifying inputs 0 Up.

P '1' - The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.

'0' - The output is configured for continuous oscillation.

W '1' - It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.

'0' - Operation shall begin within 2 ms of the command receipt.

G '1' - Operation shall be gated active by the specified input.

'0' - Gating is inactive.

L '1' - The LINESYNC based clock shall be used for the time ticks.

'0' - The MC shall be used for the time ticks.

V '1' - Indicates maximum number of configurable outputs is exceeded.

'0' - No error

Number of items - The number of entries in the frame. If 0, all outputs currently configured as complex outputs shall be disabled.

### 7.2.1.10.2 Sampling Rate

Controlling input signals shall be sampled at least once per millisecond.

### 7.2.1.10.3 Data Range

The “Number of Items” field is valid from 0 to 16. Zero means disable all Complex Output functions. Sixteen is the maximum because the most that is sent at one time is 8 enables and 8 disables. If processing a command results in more than 8 Complex Output functions being enabled, none of the command shall be implemented and the response message “V” bit shall be set to 1. If an invalid output or input number (the “G” or “W” bits being set to 1) is specified for a function, that function definition is not done by the FIOM software. It shall also not be counted towards the maximum of 8 Complex Output functions allowed. The rest of the message shall be processed. When a Complex Output function is disabled, the output is set according to the most recently received Set Outputs command. When a complex output function for an output is superseded, that is, redefined as wither another Complex Output function, or as an Input Tracking function, nothing special is done with the output. The most recent value remains until the new function changes it. The “G” bit (gating) set to 1 takes precedence over the “W” bit (triggering). If gating is ON, triggering is turned OFF, regardless of the value of the “W” bit in the command message. If a Complex Output is configured with the “G” bit set to 1 (gating) and the “P” bit set to 0 (continuous oscillation), the output is set to OFF (0) whenever the specified input changes state so that the oscillation should cease (output inactive). For a single pulse operation (“G” bit set to 1), after the
secondary duration completes the Complex Output function shall be disabled, and the output shall be set according to the most recently received Set Outputs command.

7.2.1.11 Configure Watchdog

The Configure Watchdog frames shall be used to change the software watchdog timeout value. The Command and response frames are as follows:

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 58)</td>
<td>0</td>
<td>0</td>
<td>1 1 1 0 1 0</td>
</tr>
<tr>
<td>Timeout Value</td>
<td>x</td>
<td>x</td>
<td>x x x x x x</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 186)</td>
<td>1</td>
<td>0</td>
<td>1 1 0 1 0 0</td>
</tr>
<tr>
<td>Status</td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 Y</td>
</tr>
</tbody>
</table>

7.2.1.11.1 Timeout Value

The timeout value shall be in the range between 10 to 100 ms. If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.

7.2.1.11.2 Time Out Change

On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the "Y" bit set. The response frame bit (Y) shall indicate a '1' if the watchdog has been previously set and a '0' if not.

7.2.1.12 Controller Identification

This is a legacy message command / response for PI/O modules with Datakey resident. Upon command, a response frame containing the 128 bytes of the Datakey. On NRESET transition to High or immediately prior to any interrogation of the Datakey, the PI/O shall test the presence of the Key. If absent, the PI/O Status Bit “K” shall be set and no interrogation shall take place. If a error occurs during the interrogation, Bit “K” shall be set. If "K" bit set, only the first two bytes shall be returned. The Command Response frames are as follows:
Controller Identification Command

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type Number= 59</td>
<td>0 0 1 1 1 0 1 1</td>
<td></td>
<td>Byte 1</td>
</tr>
</tbody>
</table>

Controller Identification Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type Number = 187</td>
<td>1 0 1 1 1 0 1 1</td>
<td></td>
<td>Byte 1</td>
</tr>
<tr>
<td>Status</td>
<td>0 0 0 0 0 0 0</td>
<td>K</td>
<td>Byte 2</td>
</tr>
<tr>
<td>Datakey</td>
<td>x x x x x x x</td>
<td>x</td>
<td>Bytes 3 to 130</td>
</tr>
</tbody>
</table>

**7.2.1.13 Module Identification**

The PI/O Identification command frame shall be used to request the PI/O Identification value Response of "1" for the 332 PI/O, "2" for the TS-2 Type2 PI/O, 3 for the TS-2 Type 1 PI/O. The Identification value response for ITS Cabinet SIUs and CMU shall be frame address. The command and response frames are shown as follows:

**I/O Module Identification Command**

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 60)</td>
<td>0 0 1 1 1 1 0 0</td>
<td></td>
<td>Byte 1</td>
</tr>
</tbody>
</table>

**I/O Module Identification Response**

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 188)</td>
<td>1 0 1 1 1 0 0</td>
<td></td>
<td>Byte 1</td>
</tr>
<tr>
<td>PI/O ID byte</td>
<td>x x x x x x x</td>
<td></td>
<td>Byte 2</td>
</tr>
</tbody>
</table>

**7.2.1.14 Mechanical Details**
NOTES:
1. C1S Dark Circles denote guide pin locations
2. C1S Open Circles denote guide socket locations
3. Dimension “A” shall be 0.5" minimum
4. C1S shall be M104 type
5. C11S shall be 37 pin circular plastic type
6. C1S and C11S pin assignments shown above

Figure 7-1: C1S and C11S Pin Configuration: Refer to CALTRANS TEES

7.2.2 Parallel Connection to NEMA TS-1 or TS-2 Type 2 Cabinets

7.2.2.1 Description

This PI/O shall consist of an FCU Controller, Parallel Input / Output Ports, Field Connectors and Communications Circuits. It is similar in function to the 332 style PI/O, except it provides more inputs and outputs via different physical connectors.

7.2.2.2 Front Panel

The Front Panel shall be furnished with the following:

Incoming VAC fuse protection
Four NEMA Connectors, A, B, C & D

7.2.2.3 Functional Requirements Exceptions

This PI/O shall meet all requirements identified above except that:

118 bits of input and 102 bits of output shall be provided.
Specification for inputs applies, except the voltage is +24 V in lieu of +12 V
Ground False, “0”, exceeds 16.0 VDC.
7.2.2.4 Fault Monitor and Voltage Monitor

NEMA TS-2 Controller FAULT and VOLTAGE Monitor functions (outputs to the cabinet monitor) shall be provided.

7.2.2.4.1 Monitor Logic

Two 3-input OR gates shall be provided. The gate 1 output shall be connected to Connector A, Pin A (FAULT MONITOR) and gate 2 output shall be connected to Connector A, Pin C. Any FALSE state input shall cause a gate output FALSE (+24 V) state.

7.2.2.4.2 Watchdog

The FCU Port 10, Bit 7 output shall normally change its state every 100 mS. A Watchdog Timer (WDT) circuit shall monitor the output. No state change for 2 +/- 0.1 second shall cause the circuit output to generate a FALSE (+24 VDC) output (input to gates 1 and 2). Should the FCU begin changing state, the WDT output shall return to TRUE (0 VDC) state.

7.2.2.4.3 The 5 VDC Monitor

5 VDC shall be monitored. When 5 VDC supply falls out of regulation (+/- 0.25 V), this monitor circuit shall generate a FALSE output (input to gates 1 and 2) Normal operation shall return the output state to TRUE state.

7.2.2.4.4 Fault Monitor Logic

The FCU microprocessor output shall be assigned to FAULT Monitor (input to gate 1) and another output shall be assigned to VOLTAGE MONITOR (input to gate 2).

7.2.2.4.5 Monitor Control from Application Software

CPU Port 5 SET OUTPUT COMMAND Message
OUTPUTs O78 and O79 shall be assigned to FAULT (O78) and VOLTAGE (O79). The bit logic “1” shall be FCU output FALSE.

7.2.2.4.6 Monitor Output Power Up Conditions

CPU / FCU operation at POWER UP shall be as follows:
FCU Comm Loss Flag set. FAULT & VOLTAGE MONITOR outputs set FALSE.
CPU REQUEST MODULE STATUS COMMAND Message with “E” bit set is sent to FCU to clear Comm Loss Flag and responds to CPU with “E” bit reset.
Before the Comm Loss timer expires, the SET OUTPUTS COMMAND data must be sent. In that data, the O78 and O79 logically set to “0” will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted at the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.

If the above message sequence is not followed, Comm Loss Flag shall be set (or remain) and VM & FM shall retain the FALSE output state.

Performs items 2 & 3 above User Software.

7.2.2.4.7 Communications Loss

A CPU/FCU Communications Loss during normal operation shall cause all outputs to go blank (FALSE state) and shall set the Comm Loss Flag. FM and VM outputs shall be in the FALSE state.

Figure 7-2: Connector Diagram

NOTES:

1. A = NEMA “A” Connector, Type MS-3112-22-55P
2. B = NEMA “B” Connector, Type MS-3112-22-55S
3. C = NEMA “C” Connector, Type MS-3112-24-61S
4. D = NEMA “D” Connector, Type MS-3112-24-61P
5. Spacing Between A, B, C, D Connectors = 3.0 “ min, Center to Center.

7.2.3 Mechanical Details

Connector A, B, C Pin Configurations: Refer to NEMA TS-2 Specification
Connector D Pin Configuration: Refer to CALTRANS TEES
7.2.3.1 Description
The TS-2 Type 1 PI/O provides a TS2-1 compatible interface, AC Power to the ATC, Fault Monitor Logic Output and Output Frame Byte 9 Bit 6 to the NEMA TS2 Cabinet Monitor Unit (CMU).

7.2.3.2 Front Panel
The Front Panel shall be furnished with the following:

- Incoming VAC fuse protection
- One NEMA Connector, A
- One AC Outlet for ATC Line Cord

7.2.3.3 Functional Requirements Exceptions
This PI/O shall meet all requirements specified above except:

- No C1 and C11 Connectors on the front panel of the module
- No 64 inputs / 64 outputs requirements

7.2.3.4 Parallel Connector
The parallel connector is a 10 Pin NEMA Connector A

7.2.3.5 Service Power Connection
Incoming 2070 AC Power is derived from Connector A Pin C (AC+), Pin A (AC-), and Pin H (Equipment Ground). The power is directly routed to the NEMA 5-15 Receptacle. Connector A shall intermate with a NEMA TS2 Type 1 (MS3106O-18-1S) cable.

7.2.3.6 Fault Monitor
An FCU output shall drive a open collector transistor whose output shall be routed to Connector A Pin F for use as a FAULT MONITOR Output. The transistor shall be capable of sinking 200 ma at 30 VDC.

7.2.3.7 Connector A Pin Assignment
Connectors A pin assignment: Refer to NEMA TS-2 Specification
7.3 Serial Input / Output (SI/O)

The ATC shall provide a minimum of 11 serial ports, as follows:

Guidance: The traditional (2070ATC) use of the serial ports is as follows:

- SP1: External communications, via slot A2, top connector
- SP2: External communications, via slot A2, bottom connector
- SP3: ITS Cabinet SB2, via C21S, or external communication via slot A1 top
- SP4: OS console via C50S or slot A1 bottom connector
- SP5: Field I/O communications module
- SP6: User Interface, or via C60P
- SP7: Field I/O communications via C13S connector
- SPI: Portable Memory Device (Data Key)
- ENET1: Ethernet for Network

Guidance: The planned use of the added (not on 2070ATC) serial ports is as follows:

- USB: Removable Memory Device
- ENET2: Ethernet for Local Cabinet (Expansion Rack, Upload to Laptop)

Refer to Engine Board section for a description of each serial port operation.

The ATC shall provide two internal 10/100 hubs. Ports shall be allocated as follows:

- Port 1: Internal 10/100 BPS Port to Engine Board ENET1
- Port 2: External 10/100 BPS Port to Network Backbone
- Port 3: External 10/100 BPS Port for Network Diagnostics
- Port 4: Internal 10/100 BPS Port to Engine Board ENET2
- Port 5: External 10/100 BPS Spare Port for Controller Expansion
- Port 6: External 10/100 BPS Port for Controller Diagnostics
Pictorially:

```
Advanced Transportation Controller

10/100 BPS RJ-45 Network Connection
10/100 BPS RJ-45 Network Diagnostics
10/100 BPS RJ-45 Internal Expansion
10/100 BPS RJ-45 Controller Diagnostic

10/100 BPS Hub 1
10/100 BPS Hub 2

10 MBPS ENET1
ENGINE BOARD
10 MBPS ENET2

Figure 7-3 Details of Ethernet Hub Connections
```

Hub 1:

Hub1, Port 1 connects to Engine Board ENET1, which handles the network traffic. Although ENET1 is not expected to handle 100 Mbps data streams, the ATC may find itself connected to a 100 Mbps network. Hub1 handles the speed conversion, as well as provides two RJ-45 Ethernet connectors, Port 2 and Port 3.

Port 2 provides a permanent connection to the network backbone for network communications, such as NTCIP. Port 3 does not act as a router or communications switch. Because the Engine Board cannot respond to every Ethernet packet on the trunk, the network topology must be designed to forward only packets destined for the ATC.

Port 3 is configured as an uplink for use with a “straight through” Ethernet cable. This eliminates the need to disconnect the ATC from the network to connect a laptop computer for network diagnostics, or to connect other cabinet equipment to the network.

Hub 2:

Hub2 connects to Engine Board ENET2, which communicates to local cabinet devices. Although ENET2 is not expected to handle 100 Mbps data streams, the ATC may find itself connected to a 100 Mbps network. Hub2 handles the speed conversion, as well as provides two RJ-45 Ethernet connectors, Port 5 and Port 6.
Port 5 provides a permanent connection for internal ATC expansion, such as connection to a network interface card residing in a computer rack (VME, for example). This provides a standard method to connect parallel devices such as analog to digital converters, disk storage and multiple computer boards, without specifying a particular computer bus.

Port 6 is configured as an uplink for use with a “straight through” Ethernet cable. This eliminates the need to disconnect the ATC from the network to connect a laptop computer for controller diagnostics, or to load new controller software.

7.4 Power Inputs

7.4.1 NEMA Power Inputs

Service power inputs for NEMA ATC versions shall be via the NEMA “A” connector.

7.4.2 Power Inputs, Other ATC Configurations

Service power inputs for all versions other than NEMA shall be via a three #16 conductor power cable, 3 ft minimum length, and permanently attached to the ATC with a strain relief. The end plug connector shall be a three blade NEMA 5-15P grounding plug.
NOTICE: This Electrical, Environmental, and Testing Requirements section was developed using information excerpted from NEMA TS2-2002 Traffic Controller Assemblies with NTCIP Requirements. Permissions and approvals for the reuse of the excerpted material are pending approval by NEMA.

8.1 General
This section establishes the limits of the environmental and operational conditions in which the First Article Controller Assembly will perform. This section defines the minimum test procedures which may be used to demonstrate conformance of a device type with the provisions of the standard. These test procedures do not verify equipment performance under every possible combination of environmental requirements covered by this standard. However, nothing in this testing profile shall be construed as to relieve the requirement that the equipment provided must fully comply with these standards/specifications under all environmental conditions stated herein.

Individual agencies may wish to extend the testing profile or introduce additional tests to verify compliance. (Authorized Engineering Information).

8.2 Inspection
A visual and physical inspection shall include mechanical, dimensional and assembly conformance to all parts of this standard.

8.3 Testing Certification
When required, complete quality control / final test report shall be supplied with each item. Quality control procedures shall be submitted to the purchasing agency prior to production. The test report shall indicate the name of the tester and shall be signed by a responsible manager.

The quality control procedure and test report format shall be supplied to the purchasing agency for approval upon request. The quality control procedure shall include the following, in the order shown:

- Design Acceptance testing of all supplied components.
- Physical and functional testing of all modules and items.
- Environmental testing report(s) for all equipment.
- Physical and functional testing of all items.
Separate certifications should be provided for design and production:

Design acceptance testing should be performed with a fully loaded and functional Controller Assembly meeting the requirements of this standard (Controller Assembly containing all of the Major Units necessary to provide a fully functional and operational Controller Assembly).

Production testing should be performed as part of the purchasing agency’s procurement delivery procedures and that testing should be performed at the Major Unit level. (Authorized Engineering Information).

Certain portions of the test procedures contained in this standard may cause damage to the unit (e.g. protection devices may be aged) and are not recommended for routine production testing. (Authorized Engineering Information)

### 8.4 Definitions of Major Units of the Controller Assembly

For the purpose of this section, "Major units of the Controller Assembly" shall include the Controller Unit, Application Software for implementing the desired functionality, Controller Monitor Unit (CMU), Auxiliary Monitor Unit (AMU), Serial Interface Units (SIUs), Power Distribution Unit (PDA), Switch Packs, Flasher(s), and Detector(s).

### 8.5 Environmental and Operating Requirements

The requirements (voltage, temperature, etc.) of this section shall apply in any combination.

#### 8.5.1 Voltage and Frequency

**8.5.1.1 Operating Voltage**

The nominal voltage shall be 120 VAC, unless otherwise noted.

**8.5.1.2 Operating Frequency**

The operating frequency range shall be 60 hertz (+/-3.0 hertz), unless otherwise noted.

#### 8.5.2 Transients, Power Service

The Test Unit shall maintain all defined functions when the independent test pulse levels specified in Section 8.5.2.1 on an individual unit, and Section 8.5.2.2 occur on the alternating-current power service in a Controller or assembly with protection.
8.5.2.1 High-Repetition Noise Transients
The test pulses shall not exceed the following conditions:

1. Amplitude: 300 Volts, both positive and negative polarity.
3. Repetition: 1 pulse approximately every other cycle moving uniformly over the full wave in order to sweep across 360 degrees of the line cycle once every 3 seconds.
5. Pulse Width: 10 microseconds.
6. This test is performed without protection in place or operational.

This test is considered to be a minimum test requirement for the Test Unit complying with ANSI/IEEE C62.41. Regional conditions may warrant additional testing as described in ANSI/IEEE C62.41. (Authorized Engineering Information)

8.5.2.2 Low-Repetition High-Energy Transients
The test pulses shall not exceed the following conditions:

1. Amplitude: 600 Volts (+/- 5 percent), both positive and negative polarity.
2. Energy Source: Capacitor, oil filled, 10 microfarads (+/- 10 percent), internal surge impedance less than 1 ohm.
3. Repetition: 1 discharge every 10 seconds.
5. This test is performed with protection in place and operational.

This test is considered to be a minimum test requirement for the Test Unit complying with ANSI/IEEE C62.41. Regional conditions may warrant additional testing as described in ANSI/IEEE C62.41. (Authorized Engineering Information)

8.5.3 Nondestructive Transient Immunity
The Test Unit (with protection in place and operational) shall be capable of withstanding a high energy transient having the following characteristics repeatedly applied to the
alternating current input terminals (no other power connected to terminals) without failure of the test specimen:

1. Amplitude: 1000 Volts (+/- 5 percent), both positive and negative polarity.

2. Energy Source: Capacitor, oil filled, 15 microfarads (+/- 10 percent), internal surge impedance less than 1 ohm.

3. Repetition: Applied to the Test Unit once every 2 seconds for a maximum of three applications for each polarity.

4. After the foregoing, the Test Unit shall perform all defined functions upon the application of nominal alternating current power.

This test is considered to be a minimum test requirement for the Test Unit complying with ANSI/IEEE C62.41 (100 Kiloherzt Ring Wave, the 1.2/50 microseconds – 8/20 Combination Wave and the EFT Burst) at voltages and currents specified at “Location Category B2” and at “Test Severity” level III (i.e. up to 4.0 Kilovolts, open-circuit). Regional conditions may warrant additional testing as described in ANSI/IEEE C62.41. (Authorized Engineering Information)

8.5.4 Transients, Input-Output Terminals
The Test Unit (without protection in place or operational) shall maintain all defined functions, when the test pulse occurs on the input-output terminals.

1. Amplitude: 300 Volts, both positive and negative polarity.

2. Pulse Source: 1000 ohms nominal impedance.

3. Repetition: 1 pulse per second, for a minimum of 5 pulses per selected terminal.

4. Pulse rise time: 1 microsecond.

5. Pulse width: 10 microseconds.

This test is considered to be a minimum test requirement for the Test Unit complying with ANSI/IEEE C62.41. Regional conditions may warrant additional testing as described in ANSI/IEEE C62.41. (Authorized Engineering Information)

8.5.5 Temperature and Humidity
The Test Unit shall maintain all programmed functions when the temperature and humidity ambients are within the specified limits defined herein (8.5.5.1 and 8.5.5.2).
8.5.5.1 Ambient Temperature

The operating ambient temperature range shall be from -37 degrees C to +74 degrees C. The storage temperature range shall be from -45 degrees C to +85 degrees C.

The rate of change in ambient temperature shall not exceed 18 degrees C per hour, during which the relative humidity shall not exceed 95 percent.

8.5.5.2 Humidity

The relative humidity shall not exceed 95 percent non-condensing over the temperature range of -37 degrees C to +74 degrees C.

Above +46 degrees C, constant absolute humidity shall be maintained. This will result in the relative humidities shown in Table 8-1 for dynamic testing.

<table>
<thead>
<tr>
<th>Ambient Temperature/Dry Bulb (in degrees C)</th>
<th>Relative Humidity (in percent)</th>
<th>Ambient Temperature/Wet Bulb (in degrees C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-37.0 to 1.1</td>
<td>10</td>
<td>-17.2 to 42.7</td>
</tr>
<tr>
<td>1.1 to 46.0</td>
<td>95</td>
<td>42.7</td>
</tr>
<tr>
<td>48.8</td>
<td>70</td>
<td>42.7</td>
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<td>50</td>
<td>42.7</td>
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<tr>
<td>60.0</td>
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<td>42.7</td>
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<td>42.7</td>
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<tr>
<td>71.2</td>
<td>21</td>
<td>42.7</td>
</tr>
<tr>
<td>74.0</td>
<td>18</td>
<td>42.7</td>
</tr>
</tbody>
</table>

8.6 Test Facilities

All instrumentation required in the test procedures, such as voltmeters, ammeters, thermocouples, pulse timers, etc. shall be selected in accordance with good engineering practice. In all cases where time limit tests are required, the allowance for any instrumentation errors shall be included in the limit test.

1. Variable Voltage Source: A variable source capable of supplying 20 amperes from 100 VAC to 135 VAC.

2. Environmental Chamber: An environmental chamber capable of attaining temperatures of -37 degrees C to +74 degrees C and relative humidities given in Table 8-1.

3. Transient Generator(s): Transient generator(s) capable of supplying the transients outlined in Sections 8.5.2 through 8.5.4.
8.7 Test Procedure: Transients, Temperature, Voltage, and Humidity

8.7.1 Test A: Placement in Environmental Chamber and Check-Out of Hook-Up

1. Place the test unit in the environmental chamber. Connect the test unit AC input circuit to a variable voltage power transformer, voltmeter, and transient generator. The transient generator shall be connected to the AC input circuit at a point at least 25 feet from the AC power source and not over 10 feet from the input to the test unit.

2. Connect test switches to the appropriate terminals to simulate the various features incorporated into the test unit. Place these switches in the proper position for desired operation.

3. Verify the test hook-up. Adjust the variable-voltage power transformer to 120 VAC and apply power to the test unit. Verify that the test unit goes through its prescribed startup sequence and cycles properly in accordance with the operation determined by the positioning of test switches in item 2.

Upon the satisfactory completion and verification of the test hook-up, proceed with Test B.

8.7.2 Test B: Transient Tests (Power Service)

1. Program the test unit to dwell. Verify the input voltage is 120 VAC.

2. Set the transient generator to provide high-repetition noise transients as follows:
   a. Amplitude: 300 Volts (+/- 5 percent), both positive and negative polarity.
   b. Peak Power: 2500 watts.
   c. Repetition Rate: One pulse every other cycle moving uniformly over the full wave in order to sweep once every 3 seconds across 360 degrees of line cycle.
   d. Pulse Rise Time: 1 microsecond.
   e. Pulse Width: 10 microseconds.

3. Apply the transient generator output to the AC voltage input for at least 5 minutes. Repeat this test for at least two conditions of dwell for the test unit. The test unit must continue to dwell without malfunction.
4. Program the test unit to cycle through normal operations. Turn on the transient generator (output in accordance with item 2) for 10 minutes, during which time the test unit shall continue to cycle without malfunction.

5. Set a transient generator to provide high-repetition noise transients as follows:
   a. Amplitude: 300 Volts (+/-5 percent), both positive and negative polarity.
   b. Source Impedance: Not less than 1000 ohms nominal impedance.
   c. Repetition: One pulse per second for a minimum of five pulses per selected terminal.
   d. Pulse Rise Time: 1 microsecond.
   e. Pulse Width: 10 microseconds.

   Program the test unit to dwell. Verify the input voltage is 120 VAC.

6. Apply the transient generator (output in accordance with item 5) between logic ground and the connecting cable termination of selected Field I/O input/output terminals of the test unit.

   A representative sampling of selected input/output terminations shall be tested. The test unit shall continue to dwell without malfunction.

7. Program the test unit to cycle. Turn on the transient generator (output in accordance with item 5) and apply its output to the selected Field I/O input/output terminations. The test unit shall continue to cycle without malfunction.

8. Reinstall protection and set a transient generator to provide low-repetition high-energy transients as follows:
   a. Amplitude: 600 Volts (+/-5 percent), both positive and negative polarity.
   b. Energy Discharge Source: Capacitor, oil-filled, 10 microfarads.
   c. Repetition Rate: One discharge each 10 seconds.
   d. Pulse Position: Random across 360 degrees of line cycle.

9. Program the test unit to dwell. Verify the input voltage is 120 VAC.

10. Discharge the oil-filled 10-microfarad capacitor ten times for each polarity across the AC voltage input. Repeat this test for at least two conditions of dwell. The test unit shall continue to dwell without malfunction.

11. Program the test unit to cycle through normal operations. Discharge the capacitor ten times for each polarity while the test unit is cycling, during which time the test unit shall continue to cycle without malfunction.

12. During the preceding transient tests (item 3 through 11), the test unit must continue its programmed functions.
The test unit shall not skip normal program intervals/steps or portions thereof when in normal operation; place false inputs or produce false outputs while in dwell; disrupt normal sequences in any manner; or change parameters.

13. Nondestructive Transient Immunity:
   a. Turn off the AC power input to the test unit from the variable-voltage power source.
   b. Apply the following high-energy transient to the AC voltage input terminals of the test unit (no other power connected to terminals):
      (1) Amplitude: 1000 V, both positive and negative polarity.
      (2) Peak Power Discharge: Capacitor, oil-filled, 15 microfarads.
      (3) Maximum Repetition Rate: Applied to the Controller Assembly once every 2 seconds for a maximum of three applications for each polarity.
   c. Upon completion of the foregoing, apply 120 VAC to the test unit and verify that the test unit goes through its prescribed startup sequence and cycles properly in accordance with the programmed functions. The first operation of the over-current protective device during this test shall not be considered a failure of the test unit.

NOTE—Test C through G follow the profile indicated in Figure 8-1 to demonstrate the ability of the test unit to function reliably under stated conditions of temperature, voltage, and humidity.
8.7.3 Test C: Low-Temperature Low-Voltage Tests

1. Definition of Test Conditions
   a. Environmental Chamber Door: Closed.
   b. Temperature: -37 degrees C.
   c. Low Voltage: 100 VAC.
   d. Humidity Control: Off.

2. Test Procedure: While at room temperature, adjust the input voltage to 100 VAC and verify that the test unit is still operable.
   a. With the test unit cycling through normal operations, lower the test chamber to -37 degrees C at a rate not exceeding 18 degrees C per hour. Allow the test unit to cycle for a minimum of 5 hours at -37 degrees C with the humidity controls in the off position. Then operate the test switches as necessary to determine that all functions are operable.
   b. Power shall then be removed from the test unit for a minimum period of 5 hours. Upon restoration of power, the test unit shall go through its prescribed startup sequence and then resume cycling.
   c. With the test unit at -37 degrees C and the input voltage at 100 VAC, the following items shall be evaluated against the respective standards:
      1) Given in Section 8.10 Power Interruption Tests

On satisfactory completion of this test, proceed with Test D.

8.7.4 Test D: Low-Temperature High-Voltage Tests

1. Definition of Test Conditions
   a. Environmental Chamber Door: closed.
   b. Low Temperature: -37 degrees C.
   c. High Voltage: 135 VAC.
   d. Humidity Controls: Off.

2. Test Procedure: While at -37 degrees C and with humidity controls off, adjust the input voltage to 135 VAC and allow the test unit to cycle for 1 hour. Then operate the test switches as necessary to determine that all functions are operable.
3. With the test unit at -37 degrees C and the input voltage at 135 VAC (humidity controls off), the following items shall be evaluated against the respective standards:

1) Given in Section 8.10 Power Interruption Tests

On satisfactory completion of this test, proceed to Test E.

8.7.5 Test E: High-Temperature High-Voltage Tests

1. Definition of Test Conditions
   a. Environmental Chamber Door: Closed.
   b. High Temperature: +74 degrees C.
   c. High Voltage: 135 VAC.
   d. Humidity Controls: In accordance with the humidities given in Exhibit 3-1.

2. Test Procedure—With the test unit cycling, raise the test chamber to +74 degrees C at a rate not to exceed 18 degrees C per hour. Verify the input voltage is 135 VAC.

3. Set the humidity controls to not exceed 95 percent relative humidity over the temperature range of +1.1 degrees C to +46 degrees C. When the temperature reaches +46 degrees C, readjust the humidity control to maintain constant absolute humidity; +42.7 degrees C wet bulb which results in the relative humidities shown in Table 2-1. Verify that the test unit continues to cycle satisfactory during the period of temperature increase and at established levels of relative humidity.
   a. Allow the test unit to cycle for a minimum of 15 hours at +74 degrees C and 18 percent relative humidity. Then operate the test switches as necessary to determine that all functions are operable.
   b. With the test unit at +74 degrees C and 18 percent relative humidity and the input voltage at 135 VAC, the following items shall be evaluated against the respective standards:
      1) Given in Section 8.10 Power Interruption Tests

On satisfactory completion of this test, proceed to Test F.

8.7.6 Test F: High-Temperature Low-Voltage Tests

1. Definition of Test Conditions
   a. Environmental Chamber Door: Closed.
   b. High Temperature: +74 degrees C.
   c. Low Voltage: 100 VAC.
   d. Humidity Controls: 18 percent relative humidity and +42.7 degrees C wet bulb.
2. Test Procedure: Adjust the input voltage to 100 VAC and proceed to operate the test switches to determine that all functions are operable. With the test unit at +74 degrees C and 18 percent relative humidity, +42.7 degrees C wet bulb, and the input voltage at 100 VAC, the following items shall be evaluated against the respective standards:
   1) Given in Section 8.10 Power Interruption Tests

On satisfactory completion of this test, proceed to Test G.

8.7.7 Test G: Test Termination

1. Program the test unit to cycle.
2. Adjust the input voltage to 120 VAC.
3. Set the controls on the environmental chamber to return to room temperature, +20 degrees C (+/- 5 degrees C), with the humidity controls in the off position. The rate of temperature change shall not exceed 18 degrees C per hour.
4. Verify the test unit continues to cycle through normal operations properly.
5. Allow the test unit to stabilize at room temperature for 1 hour. Proceed to operate the test switches to determine that all functions are operable.

8.7.8 Test H: Appraisal of Equipment under Test

1. A failure shall be defined as any occurrence which results in other than normal operation of the equipment. (See item 2 for details.) If a failure occurs, the test unit shall be repaired or components replaced, and the test during which failure occurred shall be restarted from its beginning.
2. The test unit is considered to have failed if any of the following occur:
   a. If the test unit skips normal program intervals/steps or portions thereof when in normal operation, places false inputs, presents false outputs, exhibits disruption of normal sequence of operations, or produces changes in parameters beyond specified tolerances, or
   b. If the test unit fails to satisfy the requirements of Section 8.7 Tests A to G, inclusive.
3. An analysis of the failure shall be performed and corrective action taken before the test unit is retested in accordance with this standard. The analysis must outline what action was taken to preclude additional failures during the tests.
4. When the number of failures exceeds two, it shall be considered that the test unit fails to meet these standards. The test unit may be completely retested after analysis of the failure and necessary repairs have been made in accordance with item 3.

5. Upon completion of the tests, the test unit shall be visually inspected. If material changes are observed which will adversely affect the life of the test unit, the cause and conditions shall be corrected before making further tests.

6. Upon satisfactory completion of all of the tests described in Sections 8.7.1 through 8.7.8, the test unit shall be tested in accordance with Section 8.8.

### 8.8 Vibration Test

Units such as the Model 2070 and certain Controller Assemblies that are controlled by specific mechanical design specifications are not subject to the tests in Sections 8.8 through 8.9.4 (Authorized Engineering Information).

#### 8.8.1 Purpose of Test

This test is intended to duplicate vibrations encountered by the test unit (individual major components) when installed at its field location.

The test unit shall be fastened securely to the vibration test table prior to the start of the test.

#### 8.8.2 Test Equipment Requirements

1. Vibration table with adequate table surface area to permit placement of the test unit.

2. Vibration test shall consist of:
   a. Vibration in each of three mutually perpendicular planes.
   b. Adjustment of frequency of vibration over the range from 5 hertz to 30 hertz.
   c. Adjustment of test table excursion (double amplitude displacement) to maintain a ‘g’ value, measured at the test table, of 0.5g; as determined by the following formula:
   \[ g = 0.0511df^2 \]
   Where:
   - \(d\) = excursion in inches
   - \(f\) = frequency in hertz
8.8.3 **Resonance [Mechanical Resonant Frequency] Search**

1. With the test unit securely fastened to the test table, set the test table for a double amplitude displacement of 0.015 inch.

2. Cycle the test table over a search range from 5 hertz to 30 hertz and back within a period of 12.5 minutes.

3. Conduct the resonant frequency search in each of the three mutually perpendicular planes.

4. Note and record the resonant frequency determined from each plane.
   a. In the event of more than one resonant frequency in a given plane, record the most severe resonance.
   b. If resonant frequencies appear equally severe, record each resonant frequency.
   c. If no resonant frequency occurs for a given plane within the prescribed range, 30 hertz shall be recorded.

8.8.4 **Endurance Test**

1. Vibrate the test unit in each plane at its resonant frequency for a period of 1 hour at amplitude resulting in 0.5g acceleration.

2. When more than one resonant frequency has been recorded in accordance with Section 8.8.4, item number 4, the test period of 1 hour shall be divided equally between the resonant frequencies.

3. The total time of the endurance test shall be limited to 3 hours, 1 hour in each of three mutually perpendicular planes.

8.8.5 **Disposition of Equipment under Test**

1. The test unit shall be examined to determine that no physical damage has resulted from the vibration tests.

2. The test unit shall be checked to determine that it is functionally operable in all modes of its prescribed operation.

3. The test unit may be removed from the test table. Upon satisfactory completion of the vibration test, proceed with the shock (impact) test described in Section 8.9.
8.9 Shock (Impact) Test

8.9.1 Purpose of Test

The purpose of this test is to determine that the test unit is capable of withstanding the shock (impact) to which it may reasonably be subjected during handling and transportation in the process of installation, repair, and replacement. It is to be noted that the test unit is not, at this time, in its shipping carton.

The test unit shall be firmly fastened to the specimen table. In each of its three planes the test unit shall be dropped from a calibrated height to result in a shock force of 10g.

8.9.2 Test Equipment Requirements

1. Shock (impact) test fixture equivalent to that suggested by the simplified sketch shown in Exhibit 3-3.

2. The test table shall have a surface area sufficient to accommodate the test unit.

3. The test table shall be calibrated and the items tested as indicated. This shock test defines the test shock to be 10g (+/- 1g).
   a. Calibration of the test equipment for these shock tests shall be measured by three accelerometers having fixed shock settings of 9g, 10g, and 11g. They shall be Inertia Switch Incorporated ST-355, or the equivalent. These devices shall be rigidly attached to the test table.
   b. Calibration of the fixture for each item to be tested shall be as follows:
      1) Place a dummy load weighing within 10 percent of the test unit on the table.
      2) Reset the three accelerometers and drop the test table from a measured height.
      3) Observe that the accelerometers indicate the following:
         a) The 9g accelerometer shall be activated.
         b) The 10g unit may or may not be actuated.
         c) The 11g unit shall not be actuated.
   c. Repeat calibration test (a) and (b) adjusting the height of the drop until, on ten successive drops, the following occurs:
      1) The 9g unit is actuated ten times.
      2) The 10g unit is actuated between four to eight times.
      3) The 11g unit is not actuated on any of the ten drops.
Figure 8-2: Shock Test Fixture
8.9.3 Test Procedure

1. The calibration height of the drop for the particular item under test as determined in Section 8.9.2 shall be used in this procedure.

2. Secure the test unit to the test table surface so that the test unit rests on one of its three mutually perpendicular planes.

3. Raise the test table to the calibrated height.

4. Release the test table from the calibrated height, allowing a free fall into the box of energy absorbing material below.

5. Repeat the drop test for each of the remaining two mutually perpendicular planes, using the same calibrated height for each drop test of the same test unit.

6. The observations of the accelerometer for the three tests of the test item shall be:
   a. The 9g unit is actuated for all three tests. (Repeat the calibration if the unit is not actuated.)
   b. The 10g unit may or may not be actuated in these tests.
   c. The 11g unit is not actuated on any drop. (If the unit is actuated, repeat the calibration only if the test unit has suffered damage.)

8.9.4 Disposition of Test Unit

1. Check the test unit for any physical damage resulting from the drop tests.

2. Check the test unit to determine that it is functionally operable in all modes of its prescribed operation.

3. Satisfactory completion of all environmental tests, including the shock (impact) is required.

8.10 Power Interruption Test Procedures

The following power interruption tests shall be conducted at low input voltage (100 VAC) and high input voltage (135 VAC) at -37 degrees C, and +74 degrees C.

8.10.1 Short Power Interruption
While the Test Unit is cycling through normal operations, remove the input voltage for a period of 475 milliseconds. Upon restoration of the input voltage, check to insure that the Test Unit continues normal operation as though no power interruption has occurred. Repeat this test three times.

8.10.2 Voltage Variation

All circuits of the Test Unit shall be subjected to slowly varying line voltage during which the Test Unit shall be subjected to line voltage that is slowly lowered from a nominal 120 VAC line voltage to 0 VAC at a rate of not greater than 2 Volts per second. The line voltage shall then be slowly raised to 100 VAC at which point the Test Unit shall resume normal operation without operator intervention. This test shall be performed at both -37 degrees C and +74 degrees C, at a nominal 120 VAC line voltage. Repeat this test three times.

8.10.3 Rapid Power Interruption

The Test Unit shall be subjected to rapid power interruption testing of the form that the power shall be off for 350 milliseconds and on for 650 milliseconds for a period of 2 minutes. Power interruption shall be performed through electromechanical contacts of an appropriate size for the load. During this testing, the controller shall function normally and shall continue normal sequencing (operation) at the conclusion of the test. This test shall be performed at both -37 degrees C and +74 degrees C, at a nominal 120 VAC line voltage. Repeat this test three times.

8.11 Controller Assembly Tests

The Controller Assembly shall perform its specified functions under the conditions set forth in this standard. This section defines the test procedures required to demonstrate the conformance of a Controller Assembly with the provisions of the standards.

In the interest of ensuring safe and reliable operation of the Controller Unit covered by these standards, the stress levels which the tests encompass are nominal Worse-Case conditions the units experience in operation. These tests are intended for Design Acceptance testing, not production testing. (Authorized Engineering Information.)

8.11.1 Test Unit

The test unit shall consist of one Controller Assembly. For Design Acceptance Testing, the Controller Assembly shall be loaded with Major Units sufficient to provide a fully functional controller system for the intended application.
8.11.2 Transients, Temperature, Voltage, and Humidity Tests

The Controller Unit shall be subjected to Transients, Temperature, Voltage, and Humidity Tests as described in section 8.7.

Figure 8-3: Overall Controller Environmental Testing Configuration

8.11.3 Power Interruption Tests

The Controller Assembly shall be subjected to Power Interruption Tests as follows:

- Short Power Interruption test as described in Section 8.10.1
- Voltage Variation test as described in Section 8.10.2
- Rapid Power Interruption test as described in Section 8.10.3

8.12 Controller Unit Tests
The individual Controller Unit shall perform its specified functions under the conditions set forth in this standard. This section defines the test procedures required to demonstrate the conformance of a Controller Unit with the provisions of the standards.

In the interest of ensuring safe and reliable operation of the Controller Unit covered by these standards, the stress levels which the tests encompass are nominal Worst-Case conditions the units experience in operation. These tests are intended for Design Acceptance testing, not production testing. (Authorized Engineering Information.)

8.12.1 Test Unit
The test unit shall consist of one Controller Unit.

8.12.2 Transients, Temperature, Voltage, and Humidity Tests
The Controller Unit shall be subjected to Transients, Temperature, Voltage, and Humidity Tests as described in Section 8.7.

8.12.3 Power Interruption Tests
The Controller Unit shall be subjected to Power Interruption Tests as follows:
- Short Power Interruption test as described in Section 8.10.1
- Voltage Variation test as described in Section 8.10.2
- Rapid Power Interruption test as described in Section 8.10.3

8.12.4 Vibration
The major units of the Controller Unit shall maintain all programmed functions and physical integrity when subjected to a vibration of 5 hertz to 30 hertz up to 0.5g's applied in each of three mutually perpendicular planes. The controller unit shall be subjected to the Vibration Test described in Section 8.8.

8.12.5 Shock (Impact)
The major units of the Controller Unit shall suffer neither permanent mechanical deformation nor any damage that renders the unit inoperable, when subjected to a shock of 10g applied in each of three mutually perpendicular planes. The controller unit shall be subjected to the Shock (Impact) Test described in Section 8.9.
9 PERFORMANCE AND MATERIAL REQUIREMENTS

9.1 General

9.1.1 Furnished Equipment

All equipment furnished in compliance to this standard under an agency’s procurement contract shall be new and unused unless that agency’s contract documents otherwise call out. Vacuum or gaseous tubes and electro-mechanical devices (unless specifically called out) shall not be used.

9.1.2 Edges

All sharp edges and corners shall be rounded.

9.1.3 Washers, Hinges, Hinge Pins

All washers, hinges and hinge pins shall be stainless steel unless otherwise specified.

9.1.4 Electrical Connections

Within the circuit of any device, module, or printed circuit board (PCB), electrical isolation shall be provided between DC ground, equipment ground and the AC grounded conductor. They shall be electrically isolated from each other by 500 mega-ohms, minimum, when tested at the input terminals with 500 VDC.

9.1.5 Component Sources

All components shall be second sourced and shall be of such design, fabrication, nomenclature or other identification as to be purchased from a wholesale distributor or from the component manufacturer, except as follows:

9.1.5.1 Special Designs

When a component is of such special design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare
duplicate component shall be furnished to the procuring agency with each twenty, or fraction thereof, components used.

9.1.5.2 Circuit Designs
The electronic circuit design shall be such that all components of the same generic type, regardless of manufacturer, shall function equally in accordance with this standard.

9.1.5.3 Operational Envelopes
No component shall be operated above 80% of its maximum rated voltage, current or power ratings. Digital components shall not be operated above 3% over their nominal voltage, current or power ratings.

9.1.5.4 Component Age
No component shall be provided under an agency’s procurement contract where the manufactured date is 3 years older than the contract award date. The design life of all components, operating for 24 hours a day and operating in their circuit application, shall be 10 years or longer.

9.1.5.5 Component Mounting
No device shall be socket mounted unless specifically called out.

9.1.5.6 Component Packaging
Encapsulation of 3 or more discrete components into circuit modules is prohibited except for transient suppression circuits, resistor networks, diode arrays, solid-state switches, optical isolators and transistor arrays. Components shall be arranged so they are easily accessible, replaceable and identifiable for testing and maintenance. Where damage by shock or vibration exists, the component shall be supported mechanically by a clamp, fastener, retainer, or hold-down bracket.

9.1.6 Capacitors
The DC and AC voltage ratings as well as the dissipation factor of a capacitor shall exceed the worst-case design parameters of the circuitry by 150%. Capacitor encasements shall be resistant to cracking, peeling and discoloration. All capacitors shall be insulated and shall be marked with their capacitance values and working voltages. Electrolytic capacitors shall not be used for capacitance values of less than 1.0 micro farad and shall be marked with polarity.
9.1.7 Resistors

Fixed carbon film, deposited carbon, or composition-insulated resistors shall conform to the performance requirements of Military Specifications MIL-R-11F or MIL-R-22684. All resistors shall be insulated. Resistance values for all discrete resistors shall be indicated by the EIA color codes, or stamped value. The value of the resistors shall not vary by more than 5% between -37 °C and 74 °C. Special ventilation or heat sinking shall be provided for all 2-watt or greater resistors. They shall be insulated from the PCB.

9.1.8 Semiconductors

All solid-state devices, except LED's, shall be of the silicon type. All transistors, integrated circuits, and diodes shall be a standard type listed by EIA and clearly identifiable. All metal oxide semiconductor components shall contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields. Device pin "1" locations shall be properly marked on the PCB adjacent to the pin.

9.1.9 Transformers and Inductors

All power transformers and inductors shall have the manufacturer's name or logo and part number clearly and legibly printed on the case or lamination. All transformers and inductors shall have their windings insulated, shall be protected to exclude moisture, and their leads color coded with an approved EIA color code or identified in a manner to facilitate proper installation.

9.1.10 Fuses

All fuses shall be 3AG Slow Blow type and resident in a holder. Fuse size rating shall be labeled on the holder. Fuses shall be easily accessible and removable without use of tools.

9.1.11 Switches

9.1.11.1 DIP switches

Dual-inline-package, quick snap switches shall be rated for a minimum of 30,000 operations per position at 50 ma, 30 VDC. The switch contact resistance shall be 100 milliohms maximum at 2 ma, 30 VDC. The contacts shall be gold over brass (or silver). Contact for VAC or 28 VDC and shall be silver over brass (or equal).
9.1.11.2 Logic switches
The switch contacts shall be rated for a minimum of one ampere resistive load at 120 VAC and shall be silver over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

9.1.11.3 Control switches
The switch contacts shall be rated for a minimum of five ampere resistive load at 120 VAC or 28 VDC and shall be gold over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

9.1.11.4 Power switches
Ratings shall be the same as for control switches, except the contact rating shall be a minimum of ten amperes at 125 VAC.

9.1.12 Wiring, Cabling, and Harnesses

9.1.12.1 Harnesses
Harnesses shall be neat, firm and properly bundled with external protection. They shall be tie-wrapped and routed to minimize crosstalk and electrical interference. Each harness shall be of adequate length to allow any conductor to be connected properly to its associated connector or termination point. Conductors within an encased harness have no color requirements.

9.1.12.2 Bundling
Wiring containing AC shall be bundled separately or shielded separately from all DC logic voltage control circuits. Wiring shall be routed to prevent conductors from being in contact with metal edges. Wiring shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

9.1.12.3 Conductor construction
All conductors shall conform to MIL-W-16878E/1 or better and shall have a minimum of 19 strands of copper. The insulation shall be polyvinyl chloride with a minimum thickness of 10 mils or greater. Where insulation thickness is 15 mils or less, the conductor shall conform to MIL-W-16878/17. Conductor color identification shall be as follows:

- Grounded AC circuits - gray or white
- Equipment ground - solid green or continuous green color with 1 or more yellow stripes.
- DC logic ground - continuous white with a red stripe.
- Ungrounded AC+ - continuous black or black with colored stripe.
9.1.13  Indicators and Character Displays

All indicators and character displays, when supplied, shall be readily visible at a radius of up to 4 feet within the cone of visibility when the indicator is subjected to 97,000 lux (9,000 foot-candles) of white light with the light source at 45 ±2 degrees to the front panel.

9.1.13.1   Range of Visibility

All indicators and character displays shall have a minimum 90 degrees cone of visibility with its axis perpendicular to the panel on which the indicator is mounted. All indicators shall be self-luminous. All indicators shall have a rated life of 100,000 hours minimum. Each LED indicator shall be white or clear when off and red when on.

9.1.13.2   LCDs

Liquid Crystal Displays (LCD), when used, shall operate at temperatures of -20 0C to +70 0C and shall not be damaged nor otherwise adversely affect unit’s operation at temperatures of -32 0C to +74 0C.

9.1.14   Connectors

All connectors shall be keyed to prevent improper insertion of the wrong connector. The mating connectors shall be designated as the connector number and male/female relationship, such as C1P (plug) and C1S (socket). The connector shall be called out base metal with minimum 0.00005 inch nickel plated with 0.000015 inch gold.

9.1.14.1   Plastic Circular and M Type Connectors

Pin and socket contacts for connectors shall be beryllium copper construction. Pin diameter shall be 0.062 inch. All pin and socket connectors shall use the AMP #601105-1 or #91002-1 contact insertion tool and the AMP #305183 contact extraction tool.

9.1.14.2   Flat Cable Connectors

All flat cable connectors shall be designed for use with 26 AWG cable; shall have dual cantilevered phosphor bronze contacts; and shall have a current rating of 1 A minimum and an insulation resistance of 5 megohms minimum.
9.1.14.3 PCB Header Post Connectors

Each PCB header post shall be 0.00394 inch square by 0.3425 inch high; shall be mounted on 0.1575 inch centers; and shall be tempered hard brass.

9.1.14.4 PCB Header Socket Connectors

Each PCB header socket block shall be nylon or diallyl phthalate. Each PCB header socket contact shall be removable, but crimp-connected to its conductor. The Contractor shall list the part number of the extraction tool recommended by its manufacturer. Each PCB header socket contact shall be brass or phosphor bronze.

9.1.15 Metal, Aluminum

If aluminum is used, Sheet shall be 63 gauge minimum thick Type 3003-H14 or Type 5052-H32 ASTM Designation B209 aluminum alloy. Rod, Bar and Extruded shall be Type 6061-T6, or equal.

9.1.16 PCB Design

No components, traces, brackets or obstructions shall be within 0.175 inch of a PC board edge (guide edges). The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all PCBs. Devices to prevent PC Board from backing out of their assembly connectors shall be provided. All screw type fasteners shall utilize locking devices or locking compounds except for finger screws, which shall be captive.

9.1.17 Tolerances

The following tolerances shall apply, except as specifically shown on the plans or in these specifications:

<table>
<thead>
<tr>
<th>Material</th>
<th>Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Metal</td>
<td>+/- 1.334 mm (0.0525 inch)</td>
</tr>
<tr>
<td>PCB</td>
<td>+/- 0.254 mm (0.010 inch)</td>
</tr>
<tr>
<td>Edge Guides</td>
<td>+/- 0.381 mm (0.015 inch)</td>
</tr>
</tbody>
</table>

9.2 Environment / Electrical

9.2.1 Operating Limits

All components shall properly operate within the following limits unless otherwise noted:
1. Applied Line Voltage: 90 to 135 VAC
2. Frequency: 60 (+/-3.0) Hertz
3. Humidity: 5% to 95%
4. Ambient Temperature: -37°C to +74°C
5. Shock - NEMA TS2 Specifications 2.1.10, 2.2.4 and Tests 2.2.9.
6. Vibration –NEMA TS2 Specifications 2.1.9, 2.2.3 and Tests 2.2.9.

9.2.2 Starting voltages

All circuits, unless otherwise noted, shall commence operation at or below 90 VAC as the applied voltage is raised from 50 to 90 VAC at a rate of 2 (+/-0.5) volts / second.

9.2.3 Transients

All equipment shall be unaffected by transient voltages normally experienced on commercial power lines. Where applicable, equipment purchased separately from the ATC cabinet (which normally is resident) will be tested for compliance in procuring agency’s accepted cabinet connected to the commercial power lines.

9.2.4 Surge Protection

The power line surge protection shall enable the equipment being tested to withstand (nondestructive) and operate normally following the discharge of a 25 microfarad capacitor, charged to plus and minus 2,000 volts, applied directly across the incoming AC line at a rate of once every 10 seconds for a maximum of 50 occurrences per test. The unit under test will be operated at 20°C (+/-5) 0C and at 120 (+/-12) VAC.

9.2.5 Line pulse testing

The equipment shall withstand (nondestructive) and operate normally when one discharge pulse of plus or minus 300 volts is synchronously added to its incoming AC power line and moved uniformly over the full wave across 360 degrees or stay at any point of Line Cycle once every second. Peak noise power shall be 5 kilowatts with a pulse rise time of 500 ns. The unit under test will be operated at 20°C (+/-5) 0C and at 120 (+/-12) VAC.

9.2.6 Generated Noise
No item, component or subassembly shall emit a noise level exceeding the peak level of 55 dBa when measured at a distance of one meter away from its surface, except as otherwise noted. No item, component or subassembly shall emit a noise level sufficient to interfere with processing and communication functions of the controller circuits.

9.3 Humidity

9.3.1 Rain Tests

Equipment shall comply only with the requirements of UL Bulletin of Research No. 23, "Rain Tests of Electrical Equipment."

9.3.2 Duration

All equipment shall resume normal operation following a period of at least 5 hours at -37°C and less than 10 percent humidity and at least 5 hours at 70°C and 22% humidity, when 90 VAC is applied to the incoming AC.

9.3.3 Relative and Ambient Temperatures

The relative humidity and ambient temperature values in the following table shall not be exceeded.

<table>
<thead>
<tr>
<th>Ambient Temperature/Dry Bulb (in °C)</th>
<th>Relative Humidity (in percent)</th>
<th>Ambient Temperature/Wet Bulb (in °C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-37.0 to 1.1</td>
<td>10</td>
<td>-17.2 to 42.7</td>
</tr>
<tr>
<td>1.1 to 46.0</td>
<td>95</td>
<td>42.7</td>
</tr>
<tr>
<td>49.8</td>
<td>70</td>
<td>42.7</td>
</tr>
<tr>
<td>54.4</td>
<td>50</td>
<td>42.7</td>
</tr>
<tr>
<td>60.0</td>
<td>38</td>
<td>42.7</td>
</tr>
<tr>
<td>65.4</td>
<td>28</td>
<td>42.7</td>
</tr>
<tr>
<td>71.2</td>
<td>21</td>
<td>42.7</td>
</tr>
<tr>
<td>74.0</td>
<td>18</td>
<td>42.7</td>
</tr>
</tbody>
</table>

All equipment shall be capable of normal operation following opening and closing of contacts in series with the applied voltage at a rate of 30 openings and closings per minute for a period of 2 minutes in duration.
10 QUALITY CONTROL

10.1 COMPONENTS –

All components shall be lot sampled to assure a consistent high conformance standard to the design specification of the equipment.

10.1.1 Subassembly, Unit Or Module

Complete electrical, environmental and timing compliance testing shall be performed on each module, unit, printed circuit or subassembly. Housing, chassis, and connection terminals shall be inspected for mechanical sturdiness, and harnessing to sockets shall be electrically tested for proper wiring sequence. The equipment shall be visually and physically inspected to assure proper placement, mounting, and compatibility of subassemblies.

10.1.2 Predelivery Repair

Any defects or deficiencies found by the inspection system involving mechanical structure or wiring shall be returned through the manufacturing process or special repair process for correction. PCB flow soldering is allowed a second time if copper runs and joints are not satisfactorily coated on the first run. Hand soldering is allowed for printed circuit repair.

10.1.3 Contractor's Testing Certification

A complete QC / final test report shall be supplied with each item. The test report shall indicate the name of the tester and shall be signed by a responsible manager. The quality control procedure and test report format shall be supplied to the Engineer for approval within 15 days following the award of the contract. The quality control procedure shall include the following:

Acceptance testing of all supplied components.
Physical and functional testing of all modules and items.
A minimum 100-hour burn-in of all equipment.
Physical and functional testing of all items.
## GLOSSARY

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>AC+</td>
<td>120 Volts AC, 60 hertz ungrounded power source</td>
</tr>
<tr>
<td>AC-</td>
<td>120 Volts AC, 60 hertz grounded return to the power source</td>
</tr>
<tr>
<td>ANSI</td>
<td>American National Standard Institute</td>
</tr>
<tr>
<td>ASCII</td>
<td>American Standard Code for Information Interchange</td>
</tr>
<tr>
<td>ASTM</td>
<td>American Society for Testing and Materials</td>
</tr>
<tr>
<td>AWG</td>
<td>American Wire Gage</td>
</tr>
<tr>
<td>C</td>
<td>Celsius</td>
</tr>
<tr>
<td>Channel</td>
<td>An information path from a discrete input to a discrete output</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>dB</td>
<td>Decibel</td>
</tr>
<tr>
<td>dBa</td>
<td>Decibels above reference noise, adjusted</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DIN</td>
<td>Deutsche Industrie Norm [German]</td>
</tr>
<tr>
<td>DMA</td>
<td>Direct Memory Access</td>
</tr>
<tr>
<td>EIA</td>
<td>Electronic Industries Association</td>
</tr>
<tr>
<td>EMI</td>
<td>Electro Magnetic Interference</td>
</tr>
<tr>
<td>ETL</td>
<td>Electrical Testing Laboratories, Inc.</td>
</tr>
<tr>
<td>FLASH</td>
<td>A Memory Device with nonvolatile, electrically erasable, programmable, 100K read/write minimum cycles and fast access time features</td>
</tr>
<tr>
<td>FPA</td>
<td>Front Panel Assembly</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
</tr>
<tr>
<td>Term</td>
<td>Definition</td>
</tr>
<tr>
<td>------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>ISO</td>
<td>International Standards Organization</td>
</tr>
<tr>
<td>Jumper</td>
<td>A means of connecting/disconnecting two or more conductive by soldering/ desoldering a conductive wire or by PCB post jumper</td>
</tr>
<tr>
<td>LED</td>
<td>Light Emitting Diode</td>
</tr>
<tr>
<td>lsb</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Byte</td>
</tr>
<tr>
<td>MB</td>
<td>MegaByte</td>
</tr>
<tr>
<td>Module</td>
<td>A functional unit that plugs into an assembly</td>
</tr>
<tr>
<td>msb</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Byte</td>
</tr>
<tr>
<td>NA</td>
<td>Presently Not Assigned. Cannot be used by the contractor for other purposes</td>
</tr>
<tr>
<td>NEMA</td>
<td>National Electrical Manufacturer's Association</td>
</tr>
<tr>
<td>NETA</td>
<td>National Electrical Testing Association, Inc.</td>
</tr>
<tr>
<td>nlsb</td>
<td>Next Least Significant Bit</td>
</tr>
<tr>
<td>NLSB</td>
<td>Next Least Significant Byte</td>
</tr>
<tr>
<td>nmsb</td>
<td>Next Most Significant Bit</td>
</tr>
<tr>
<td>NMSB</td>
<td>Next Most Significant Byte</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>SCC</td>
<td>Serial Communications Controller</td>
</tr>
<tr>
<td>SCI</td>
<td>Serial Communications Interface</td>
</tr>
<tr>
<td>SDLC</td>
<td>Synchronous Data Link Control</td>
</tr>
<tr>
<td>TOD</td>
<td>Time Of Day Clock</td>
</tr>
<tr>
<td>TTL</td>
<td>Transistor-Transistor Logic</td>
</tr>
<tr>
<td>Acronym</td>
<td>Definition</td>
</tr>
<tr>
<td>---------</td>
<td>------------</td>
</tr>
<tr>
<td>UL</td>
<td>Underwriter's Laboratories, Inc.</td>
</tr>
<tr>
<td>VAC</td>
<td>Voltage Alternating Current</td>
</tr>
<tr>
<td>VDC</td>
<td>Voltage Direct Current</td>
</tr>
<tr>
<td>VME</td>
<td>Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2</td>
</tr>
<tr>
<td>WDT</td>
<td>Watchdog Timer: A monitoring circuit, external to the device watched, which senses an Output Line from the device and reacts</td>
</tr>
</tbody>
</table>