A User Comment Draft of the
Advanced Transportation Controller Joint Committee

ATC 2070 Standard v03.01

Advanced Transportation Controller (ATC)
Standard for the Model 2070 Controller

June 13, 2011

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## CHANGE HISTORY

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</tr>
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</table>
FOREWORD

The Advanced Transportation Controller (ATC) standards effort began with the Federal Highway Administration (FHWA) gathering together a group of users interested in furthering the development of open architecture hardware and software standards to meet the future needs of Intelligent Transportation Systems (ITS). The ATC users group gained the support of three Standard Development Organizations (SDOs): the Institute of Transportation Engineers (ITE), the American Association of State Highway and Transportation Officials (AASHTO) and the National Electrical Manufacturer’s Association (NEMA). In July, 1999, a formal agreement was reached among NEMA, ITE and AASHTO to jointly develop, approve and maintain the ATC standards. An ATC Joint Committee (JC), made up of representatives of each of the SDOs, was formed to oversee and direct the work items under the ATC program with Working Groups (WGs) to produce the standards. The first official meeting of the ATC Controller WG was in September, 1999.

In the early 1990s, the State of California Department of Transportation (Caltrans) began a project to develop a specification for a Model 2070 traffic controller as a replacement for the Model 170 controller series. This work had matured enough so that the ATC JC elected to include the Model 2070 controller in the ATC family of standards. Portions of the Caltrans Transportation Electrical Equipment Specifications (TEES) 1999 plus errata that applied to the Model 2070 controller were generalized into the national standard ATC 2070 v01.05. This standard was an official standard of the ATC JC but it is now out of date and not recommended for new designs. The term “Type 2070” was used in earlier versions of the ATC 2070 Standard. This has been replaced with the term “Model 2070” to be consistent with the Caltrans TEES.

ATC 2070 v03 represents the latest and most widely used Model 2070 elements. In an effort to maintain harmony with the Caltrans specifications and consistency in deployments nationally, sections of this standard and detailed drawings have been extracted directly from the Caltrans TEES 2009 plus published errata. Some editorial, formatting changes, and section numbering have been made as deemed appropriate by the ATC Controller WG.

Inquiries, comments or proposed changes to this standard should be submitted to:

   ITS Standards Manager
   Institute of Transportation Engineers
   1627 I (eye) Street, NW, Suite 600
   Washington, DC 20006

   Voice:  (202) 785-0060
   Fax:    (202) 785-0609
   Email:  standards@ite.org
1 INTRODUCTION

This section provides an introduction for this document. It includes sections on “Purpose;” “Scope;” “Definitions, Acronyms, and Abbreviations;” “References;” and “Overview.

1.1 Purpose

The Advanced Transportation Controller (ATC) Standards are intended to provide an open architecture hardware and software platform that can support a wide variety of Intelligent Transportation Systems (ITS) applications including traffic management, safety, security and other applications. The ATC Standards are being developed and maintained under the direction of the ATC Joint Committee (JC) which is made up of representatives from the American Association of State Highway and Transportation Officials (AASHTO), the Institute of Transportation Engineers (ITE) and the National Electrical Manufacturers Association (NEMA).

This standard defines the ATC Model 2070 transportation controller (ATC 2070). It has been prepared by the ATC Controller Working Group (WG), a technical subcommittee of the ATC JC. It establishes a common understanding of the specifications for the ATC 2070 for:

a) The local, state and federal transportation agencies who specify and use ATC 2070 equipment;
b) Manufacturers who produce ATC 2070 equipment;
c) Software developers who develop application programs for ATC 2070 equipment; and
d) The public who benefit from the application programs that run on ATC 2070 equipment and who directly or indirectly pays for these products.

1.2 Scope

The ATC 2070 is an environmentally hardened computer designed for transportation related field applications. It is compatible with the major transportation field cabinet systems in use today including Caltrans Model 332 (type), NEMA TS 1, NEMA TS 2 Type 1 and Type 2, and ITS Cabinets. See Section 1.4 References for the documents that describe the various cabinet systems. The ATC 2070 has specific requirements on internal and physical characteristics to ensure uniformity across manufacturers. It features a multi-tasking operating system, module level interchangeability and expandability so that modules can be added after the initial purchase to provide more features. Its open architecture design allows software to be purchased independently of the hardware. This enables the ATC 2070 to be used for traditional traffic applications such as traffic control, data collection, and ramp metering or any other applications requiring an on-street computing platform.

1.3 Definitions, Acronyms, and Abbreviations

<p>| 170  | A traffic control device, formally a Model 170 Controller, first deployed in the early 1980s. Featured replaceable modules and an open architecture that allowed development of third party application software. The term 170 cabinet is sometimes a used referring to a Caltrans 332 (type) of cabinet system. |
| 210  | An element of a Caltrans 332 (type) of cabinet system, formally a Model 210 Monitor. |
| A    | Amperes |
| AASHTO | American Association of State Highway and Transportation Officials |
| AC   | Alternating Current |
| AC+  | 120 VAC, 60 hertz ungrounded power source |
| AC-  | 120 VAC, 60 hertz grounded return to the power source |</p>
<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Agency</td>
<td>Purchasing Government Agency</td>
</tr>
<tr>
<td>ANSI</td>
<td>American National Standard Institute</td>
</tr>
<tr>
<td>API</td>
<td>Application Program Interface</td>
</tr>
<tr>
<td>ASCII</td>
<td>American Standard Code for Information Interchange</td>
</tr>
<tr>
<td>Assembly</td>
<td>A complete machine, structure or unit of a machine that was manufactured by fitting together parts and/or modules</td>
</tr>
<tr>
<td>ASTM</td>
<td>American Society for Testing and Materials</td>
</tr>
<tr>
<td>ATC</td>
<td>Advanced Transportation Controller</td>
</tr>
<tr>
<td>AWG</td>
<td>American Wire Gage</td>
</tr>
<tr>
<td>bps</td>
<td>Bits per second</td>
</tr>
<tr>
<td>Big Endian</td>
<td>The sequencing of byte order in memory such that the most significant byte is stored at the lowest memory address, with the next byte in significance stored at the next memory location, and so on.</td>
</tr>
<tr>
<td>C</td>
<td>Celsius</td>
</tr>
<tr>
<td>C Language</td>
<td>The ANSI C Programming Language</td>
</tr>
<tr>
<td>Cabinet</td>
<td>An outdoor enclosure generally housing the controller unit and associated equipment.</td>
</tr>
<tr>
<td>Certificate of Compliance</td>
<td>A certificate signed by the manufacturer of the material or the manufacturer of assembled materials stating that the materials involved comply in all respects with the requirements of the specifications.</td>
</tr>
<tr>
<td>Channel</td>
<td>An information path from a discrete input to a discrete output</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>Component</td>
<td>Any electrical or electronic device</td>
</tr>
<tr>
<td>Contractor</td>
<td>The person or persons, manufacturer, firm, partnership, corporation, vendor or combination thereof, who have entered into a contract with the Agency, as party(ies) of the second part or legal representative.</td>
</tr>
<tr>
<td>Controller Unit</td>
<td>That portion of the controller assembly devoted to the operational control of the logic decisions programmed into the assembly</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>CRC</td>
<td>Cyclic Redundancy Check</td>
</tr>
<tr>
<td>CTS</td>
<td>Clear To Send</td>
</tr>
<tr>
<td>DAT Program</td>
<td>The Agency's Diagnostic and Acceptance Test Program</td>
</tr>
<tr>
<td>Daughter Board</td>
<td>(from TechEncyclopedia) A Printed Circuit Board that plugs into another Printed Circuit Board to augment its capabilities</td>
</tr>
<tr>
<td>dB</td>
<td>Decibel</td>
</tr>
<tr>
<td>dBa</td>
<td>Decibels above reference noise, adjusted</td>
</tr>
<tr>
<td>dBm</td>
<td>Decibels referenced to 1 milliwatt</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DCE</td>
<td>Data Communications Equipment</td>
</tr>
<tr>
<td>DIN</td>
<td>Deutsche Industrie Norm</td>
</tr>
</tbody>
</table>
DST  
Daylight Saving Time

DTE  
Data Terminal Equipment

DPST  
Double Pole Single Throw

EG  
Equipment Ground

EIA  
Electronic Industries Association

EMI  
Electro Magnetic Interference

Engineer  
The Agency director, acting either directly or through properly authorized agents, such agents acting within the scope of the particular duties delegated to them

EPROM  
Ultraviolet Erasable, Programmable, Read Only Memory Device

EEPROM  
Electrically Erasable, Programmable, Read Only Memory Device

Equal  
Connectors: comply to physical dimensions, contact material, plating and method of connection. Devices: conforming to function, pin out, electrical and operating parameter requirements, access times and interface parameters of the specified device

ETL  
Electrical Testing Laboratories, Inc.

FCU  
Field I/O Controller Unit.

F  
Fahrenheit

F  
Farad

Firmware  
A computer program or software stored permanently in PROM, EPROM, ROM or semi-permanently in EEPROM

FLASH  
An IC Memory Device with nonvolatile, electrically erasable, programmable, 100,000 read/write minimum cycles and fast access time features

FPA  
Front Panel Assembly

H  
Henry

HDLC  
High-Level Data Link Control

Hex  
Hexadecimal

Hg  
Mercury

Hz  
Hertz

IC  
Integrated Circuit

I.D.  
Identification

IEEE  
Institute of Electrical and Electronics Engineers

in  
Inches

IP  
Internet Protocol

IPC  
Association of Connecting Electronics Industries

IPI  
Initial Protocol Identifier

ISP  
Internet Support Package
<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISO</td>
<td>Short for “Isolated” and signifies that two or more power supplies each have different reference grounds.</td>
</tr>
<tr>
<td>ISO/IEC</td>
<td>International Standards Organization</td>
</tr>
<tr>
<td>ITE</td>
<td>Institute of Transportation Engineers</td>
</tr>
<tr>
<td>ITS</td>
<td>Intelligent Transportation Systems</td>
</tr>
<tr>
<td>Jumper</td>
<td>A means of connecting/disconnecting two or more conductive points by soldering/desoldering a conductive wire.</td>
</tr>
<tr>
<td>kB</td>
<td>Kilobytes</td>
</tr>
<tr>
<td>Laboratory</td>
<td>The established laboratory of the Agency or other laboratories authorized by the Agency to test materials involved in the contract</td>
</tr>
<tr>
<td>LED</td>
<td>Light Emitting Diode</td>
</tr>
<tr>
<td>LOGIC</td>
<td>Negative Logic Convention (Ground True) State</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Byte</td>
</tr>
<tr>
<td>Isb</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>M</td>
<td>Mega</td>
</tr>
<tr>
<td>m</td>
<td>Milli</td>
</tr>
<tr>
<td>MB</td>
<td>Megabyte</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Byte</td>
</tr>
<tr>
<td>msb</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>MPU</td>
<td>Microprocessor Unit</td>
</tr>
<tr>
<td>MIL</td>
<td>Military Specifications</td>
</tr>
<tr>
<td>MODEM</td>
<td>Modulation/Demodulation Unit</td>
</tr>
<tr>
<td>Module</td>
<td>A functional unit that plugs into an assembly</td>
</tr>
<tr>
<td>Motherboard</td>
<td>A printed circuit connector interface board with no active or passive components</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>MOV</td>
<td>Metal-Oxide Varistor</td>
</tr>
<tr>
<td>MS</td>
<td>Military Standards</td>
</tr>
<tr>
<td>N.C.</td>
<td>Normally closed contact</td>
</tr>
<tr>
<td>N.O.</td>
<td>Normally open contact</td>
</tr>
<tr>
<td>NA</td>
<td>Presently Not Assigned. Cannot be used by the manufacturer for other purposes.</td>
</tr>
<tr>
<td>NEMA</td>
<td>National Electrical Manufacturer’s Association</td>
</tr>
<tr>
<td>NETA</td>
<td>National Electrical Testing Association, Inc.</td>
</tr>
<tr>
<td>n</td>
<td>nano</td>
</tr>
<tr>
<td>NLSB</td>
<td>Next Least Significant Byte</td>
</tr>
<tr>
<td>nlsb</td>
<td>Next Least Significant Bit</td>
</tr>
<tr>
<td>NMSB</td>
<td>Next Most Significant Byte</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Definition</td>
</tr>
<tr>
<td>--------------</td>
<td>------------</td>
</tr>
<tr>
<td>nmsb</td>
<td>Next Most Significant Bit</td>
</tr>
<tr>
<td>NTCIP</td>
<td>National Transportation Communication for ITS Protocol</td>
</tr>
<tr>
<td>OS-9</td>
<td>Real-time Operating System from Radisys Corp.</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PDA</td>
<td>Power Distribution Assembly</td>
</tr>
<tr>
<td>PLA/PAL</td>
<td>Programmable Array Logic Device</td>
</tr>
<tr>
<td>PMPP</td>
<td>Point-to-Multi-Point Protocol</td>
</tr>
<tr>
<td>ppm</td>
<td>Parts per million</td>
</tr>
<tr>
<td>PPP</td>
<td>Point-to-Point Protocol</td>
</tr>
<tr>
<td>PROM</td>
<td>Programmable Read-Only Memory</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>RAM</td>
<td>Random Access Memory</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RMS</td>
<td>Root-Mean-Square</td>
</tr>
<tr>
<td>ROM</td>
<td>Read Only Memory</td>
</tr>
<tr>
<td>RTS</td>
<td>Request to Send</td>
</tr>
<tr>
<td>RX</td>
<td>Receive</td>
</tr>
<tr>
<td>RXD</td>
<td>Receive Data</td>
</tr>
<tr>
<td>SCC</td>
<td>Serial Communications Controller</td>
</tr>
<tr>
<td>SDLC</td>
<td>Synchronous Data Link Control</td>
</tr>
<tr>
<td>s</td>
<td>second</td>
</tr>
<tr>
<td>SS</td>
<td>Second-sourced. Produced by more than one manufacturer.</td>
</tr>
<tr>
<td>Shunt</td>
<td>A means of connecting/disconnecting two conductive points on a solderless PCB post heater.</td>
</tr>
<tr>
<td>SR</td>
<td>ACIA Status Register</td>
</tr>
<tr>
<td>SRAM</td>
<td>Static Random Access Memory Device</td>
</tr>
<tr>
<td>SW</td>
<td>Switch</td>
</tr>
<tr>
<td>TB</td>
<td>Terminal Block</td>
</tr>
<tr>
<td>TIA</td>
<td>Telecommunications Industry Association</td>
</tr>
<tr>
<td>TOD</td>
<td>Time-of-Day</td>
</tr>
<tr>
<td>Triac</td>
<td>Silicon-Controlled Rectifier which controls power bilaterally in an AC switching circuit</td>
</tr>
<tr>
<td>TTL</td>
<td>Transistor-Transistor Logic</td>
</tr>
<tr>
<td>TSD</td>
<td>Thumb Screw Device. A retractable screw fastener with projecting stainless steel screw, spring and natural aluminum knob finish</td>
</tr>
<tr>
<td>TX</td>
<td>Transmit</td>
</tr>
<tr>
<td>TXC</td>
<td>Transmit Clock</td>
</tr>
</tbody>
</table>
TXCI  Transmit Clock Input
TXCO  Transmit Clock Output
TXD  Transmit Data
µ  Micro
UL  Underwriter’s Laboratories, Inc.
VAC  Voltage Alternating Current
VDC  Voltage Direct Current
VME  Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2
X  Number Value
XX  Manufacturer’s Option
WDT  Watchdog Timer. A timing/monitoring circuit, external to the device being monitored, which senses an Output Line from the device and reacts.

1.4 References

“ATC Standard for the Type 2070 Controller v01.05,” ATC JC, 29 March 2001. Available from the Institute of Transportation Engineers.


“NEMA Standards Publication TS 2-2003 v02.06 Traffic Controller Assemblies with NTCIP Requirements.” Available from the National Electrical Manufacturers Association.

1.5 Overview

This standard is made up of three sections and appendices. Section 1, “Introduction,” provides an overview of the entire document. Section 2, “Overall Description,” provides the background information and context necessary for the requirements. Section 3, “Specific Requirements,” contains the detailed requirements and specifications for the ATC 2070.
2 OVERALL DESCRIPTION

This section provides an overall description for the ATC 2070 controller. It includes sections on “Product Perspective;” “Product Functions;” “User Characteristics;” “Constraints;” “Assumptions and Dependencies;” and “Apportioning of Requirements.”

2.1 Product Perspective

The ATC 2070 was originally designed as a replacement for 170 controllers whose basic design was deployed in the early 1980s. Users needed more computing power deployed in the field to provide for more sophisticated application programs and a controller that would support other types of cabinet systems.

The ATC 2070 has specific requirements on internal and physical characteristics to ensure uniformity across manufacturers. It features a multi-tasking operating system, module level interchangeability and expandability so that modules can be added after the initial purchase to provide more features. Its open architecture design allows software to be purchased independently of the hardware. This enables the ATC 2070 to be used for traditional traffic applications such as traffic control, data collection, and ramp metering or any other applications requiring an on-street computing platform. Figure 1 and Figure 2 show an example 2070 configuration from the front and back views respectively.

As a national specification, additional modules were created so that the ATC 2070 could be used in the most prevalent cabinet systems including the Caltrans Model 332 (type), NEMA TS 1, NEMA TS 2 Type 1 and Type 2, and ITS Cabinets. This includes cabinet systems that require discrete wiring throughout the cabinet (i.e. Model 332 (type), NEMA TS 1 and NEMA TS 2 Type 2) and cabinet systems that have serial-based communications to the elements of the cabinet (i.e. NEMA TS 2 Type 1 and ITS Cabinets). Figure 3 illustrates the ATC 2070 being rack mounted in a Model 332 cabinet system and shelf mounted in a NEMA TS 2 Type 1 cabinet system.

![Figure 1. Front view of the Model 2070 controller unit with a 2070-3B Front Panel.](image-url)
Figure 2. Rear view of a Model 2070 controller unit with various plug in modules.

Figure 3. 2070 Controllers used in rack mount and shelf mount cabinet systems.
2.2 Product Functions

The ATC 2070 is an environmentally hardened computer designed for transportation related field applications. It features a multi-tasking operating system that can be used to host any application to the limits of memory and processing power of the unit. The functions of the product are that of the operational application program(s) loaded and running on the controller.

2.3 User Characteristics

For the purposes of this standard, the users of the ATC 2070 are listed below.

- Traffic Maintenance Technicians – These individuals are required to troubleshoot and repair ATC 2070 failures through wiring, part, module or assembly replacement. They may be trained by the agency or participate in International Municipal Signal Association (IMSA) courses for certification in the maintenance and repair of traffic management devices.

- Traffic Operations Engineers and Staff – These individuals are responsible for specifying the ATC 2070 and its internal configuration based on standardized elements (e.g. modules and parts). They create the procurement documents.

- Traffic Engineers / Transportation Supervisors – These individuals have knowledge of traffic control policies and practices. They establish the processes and procedures for the use of field location equipment. They typically understand how to program and configure field location equipment although they may not perform this task operationally. They are responsible for the overall performance of the traffic management infrastructure. They are the end user of the ATC 2070.

- Communications Engineers – These individuals understand computer based communications systems, networking, wired and wireless connectivity, peer-to-peer and central-to-field communications, etc. They are also responsible for IT policies, network performance, network security and troubleshooting communications issues.

2.4 Constraints

The ATC 2070’s modular architecture is a catalyst for innovation and extension. There are numerous modules at various levels of utilization nationally that have been designed to operate within the ATC 2070 architecture. The modules identified in this standard are only those that the ATC WG has determined are nationally accepted and have demonstrated interchangeability with ATC 2070 controllers from multiple manufacturers.

2.5 Assumptions and Dependencies

There are no other assumptions or dependencies than those that may be stated in other sections of this standard.

2.6 Apportioning of Requirements

There are no requirements apportioned to a time period or specific plan within this standard. The requirements for any given deployment of this standard may vary according the configurations required by the procuring user or agency. See the introduction to Section 3 for a discussion on applicable requirements.
3 SPECIFIC REQUIREMENTS

This section provides the specific requirements for the ATC 2070 controller. It includes subsections focused on key elements of the ATC 2070. The requirements within these sections are described below.

- Sections 3.1 through 3.7 define requirements that apply to the entire controller unit. These requirements apply to all ATC 2070 units covered under this standard.
- Sections 3.8 and 3.17 define unit level naming conventions used. These requirements are dependent on the specific procurement configuration.
- Section 3.9 defines requirements for the CPU Module. These requirements apply to all ATC 2070 units covered under this standard.
- Sections 3.10, 3.18 and 3.20 define requirements for Field I/O Devices. These requirements are dependent on the specific procurement configuration.
- Section 3.11 defines requirements for Front Panels. These requirements are dependent on the specific procurement configuration.
- Sections 3.12 and 3.19 define the requirements for the Power Supply Modules. These requirements are dependent on the specific procurement configuration.
- Section 3.13 defines requirements for a VME Cage Assembly. These requirements are dependent on the specific procurement configuration.
- Sections 3.14 through 3.16 define requirements for Communications Modules. These requirements are dependent on the specific procurement configuration.
3.1 General Requirements

3.1.1 Section Conflict

In case of conflicting requirements between sections, specific requirements within Section 3.8 or higher shall govern over Sections 3.1 through 3.7.

3.1.2 Furnished Equipment

All furnished Equipment shall be new and unused. Vacuum or gaseous tubes and electro-mechanical devices (unless specifically called out) shall not be used.

3.1.3 Interchangeability

The following assemblies and their respective associated devices shall electrically and mechanically intermate and be compatible with each other:

<table>
<thead>
<tr>
<th>ASSEMBLIES</th>
<th>ASSOCIATED DEVICES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model 2070 Controller Unit</td>
<td>Cabinet Models 332, 334, 336 &amp; ITS</td>
</tr>
<tr>
<td></td>
<td>Model 2070-1 CPU Module</td>
</tr>
<tr>
<td></td>
<td>Model 2070-2 Field I/O Module</td>
</tr>
<tr>
<td></td>
<td>Model 2070-3 Front Panel Assembly</td>
</tr>
<tr>
<td></td>
<td>Model 2070-4 Power Supply</td>
</tr>
<tr>
<td></td>
<td>Model 2070-5 VME Cage Assembly</td>
</tr>
<tr>
<td></td>
<td>Model 2070-6 Serial Comm Module</td>
</tr>
<tr>
<td></td>
<td>Model 2070-7 Serial Comm Module</td>
</tr>
<tr>
<td>Model 2070-N1 Controller Unit</td>
<td>Model 2070 Controller Unit</td>
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<tr>
<td></td>
<td>Model 2070-8 NEMA Module</td>
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<tr>
<td></td>
<td>Model 2070-2B Field I/O Module</td>
</tr>
<tr>
<td></td>
<td>Model 2070-4N Field I/O Module</td>
</tr>
<tr>
<td>Model 2070-N2 Controller Unit</td>
<td>Model 2070 Controller Unit</td>
</tr>
<tr>
<td></td>
<td>Model 2070-2N Field I/O Module</td>
</tr>
<tr>
<td></td>
<td>Model 2070-4N Power Supply Module</td>
</tr>
</tbody>
</table>

3.1.4 Documentation

3.1.4.1 Manual

Two copies of Manual Documentation shall be supplied for each item purchased up to 200 manuals per order. The manual shall be bound in durable covers made of either 65-pound stock paper or clear plastic. The manual shall be printed on 8.5 in by 11 in paper, with the exception that schematics, layouts, parts lists and plan details may be on 11 in by 17 in sheets, with each sheet neatly folded to 8.5 in by 11 in size. Manual text font shall be ARIAL BOLD, size 12. Text characters shall be no more than 10 characters per 1 in and 7 lines per 1 in, with the exception of schematic text, which shall be no more than 18 characters per 1 in and 11 lines per 1 in.

3.1.4.2 Parts Listed

The title, device name, date, serial numbers and revision numbers of equipment covered by the manuals shall be printed on the front cover of the manuals. The manual shall be separated into two volumes; volume one shall be labeled as Operating Manual and volume two shall be labeled as Electrical/Mechanical Drawings.
Volume one of the Manual shall include a table of contents and items 2 through 9 and Volume two shall include a table of contents and items 10 through 12 in order as listed:

<table>
<thead>
<tr>
<th>Item #</th>
<th>Section #</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>N/A</td>
<td>Table of Contents</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>Glossary</td>
</tr>
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<td>3</td>
<td>2</td>
<td>General Description</td>
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<td>General Characteristics</td>
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<td>5</td>
<td>4</td>
<td>Installation</td>
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<td>6</td>
<td>5</td>
<td>Adjustments</td>
</tr>
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</table>
| 7      | 6         | Theory of Operation  
|        |           | a. Systems Description (include block diagram). 
|        |           | b. Detailed Description of Circuit Operation. |
| 8      | 7         | Maintenance  
|        |           | a. Preventive Maintenance. 
|        |           | b. Trouble Analysis. 
|        |           | c. Trouble Shooting Sequence Chart. 
|        |           | d. Wave Forms. 
|        |           | e. Voltage Measurements. 
|        |           | f. Alignment Procedures. |
| 9      | 8         | Parts List (include circuit and board designation, part type and class, power rating, component manufacturer, mechanical part manufacturer, data specification sheets for special design components and original manufacturer’s part number). |
| 10     | 9         | Electrical Interconnection Details & Drawings. |
| 11     | 10        | Schematic and Logic Diagram. |
| 12     | 11        | Assembly Drawings and a pictorial diagram showing physical locations and identification of each component or part. |

3.1.4.3 Draft

A preliminary Draft of the Manual shall be submitted to the Engineer for approval prior to final printing.

3.1.5 Packaging

Each item delivered shall be individually packed in its own shipping container. When loose styrofoam is used for packing the item, the item shall be sealed in a conductive plastic bag to prevent direct contact with the styrofoam.

3.1.6 Delivery

Each item delivered for testing shall be complete, including manuals, and ready for testing.

3.1.7 Metal Edges

All sharp edges and corners shall be rounded and free of any burrs.

3.1.7.1 Aluminum
Aluminum sheets shall be Type 3003-H14 or Type 5052-H32 ASTM Designation B209 aluminum alloy. Rod, Bar and Extruded shall be Type 6061-T6, or equal.

3.1.7.2 Stainless Steel

Stainless Steel Sheets shall be annealed or one-quarter-hard complying with the ASTM Designation: A666 for Type 304, Grades A or B, stainless steel sheet.

3.1.7.3 Cold Rolled Steel

Cold Rolled Steel Sheets, Rods, Bars and Extruded shall be Type 1018/1020.

3.1.7.3.1 Plating

All cold roll steel shall be plated. All plating shall be either cadmium plating meeting the requirements of Federal Specification QQ-P-416C, Type 2 Class I or zinc plating meeting the requirements of ASTM B633-85 Type II SC4.

3.1.8 Mechanical Hardware

All hardware bolts, nuts, washers, screws, hinges and hinge pins shall be stainless steel unless otherwise specified.

3.1.8.1 TSD Identifiers

The TSDs used in this standard shall be identified as follows:

- TSD #1  8-32 SOUTHCO #47-62-301-20 or equal
- TSD #2  8-32 SOUTHCO #47-62-301-60 or equal. TSD No. 2 shall be flat black.
- TSD #3  M3 SOUTHCO #47-81-181-10 or equal.

3.1.9 Electrical Isolation

Within the circuit of any device, module, or PCB, Electrical Isolation shall be provided between DC logic ground, EG and the AC- conductor. They shall be electrically isolated from each other by 500 MΩ, minimum, when tested at the input terminals with 100 VDC.

3.1.10 Daughter Boards

Keyboards and LCD/LED Displays are considered daughter boards. Daughter boards shall be mechanically secured with four spacers / metal screws depending on the area supported. Connectors shall be either Flat Cable or PCB Headers. Components are allowed to be mounted under the daughter board.
3.2 Components

3.2.1 General

All components shall be second sourced and shall be of such design, fabrication, nomenclature or other identification as to be purchased from a wholesale distributor or from the component manufacturer, except as follows:

3.2.1.1 Special Design

When a component is of such Special Design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used.

3.2.1.2 Electronic Circuit

The Electronic Circuit design shall be such that all components of the same generic type, regardless of manufacturer, shall function equally in accordance with the specifications.

3.2.2 Electronic Components

3.2.2.1 Socket Mounted

No device shall be Socket Mounted unless specifically called out within this standard or requested and approved by the procuring agency.

3.2.2.2 Rated Power

No component shall be operated above 80% of its maximum Rated Voltage, current or power ratings. Digital components shall not be operated above 3% over their nominal voltage, current or power ratings.

3.2.2.3 Manufactured Date

No component shall be provided where the Manufactured Date is 3 years older than the contract award date. The design life of all components, operating continuously (24 hours a day, 365 days per year) in their circuit application, shall be 10 years or longer.

3.2.2.4 Encapsulation

Encapsulation of 2 or more discrete components into circuit modules is prohibited except for transient suppression circuits, resistor networks, diode arrays, solid-state switches, optical isolators, transistor arrays and termination networks. Components shall be arranged so they are easily accessible, replaceable and identifiable for testing and maintenance. Where damage by shock or vibration exists, the component shall be supported mechanically by a clamp, fastener, retainer, or hold-down bracket.

3.2.2.5 Contractor

The Contractor shall submit detailed engineering technical data on all components at the request of the Engineer. A letter from the component manufacturer shall be submitted with the detailed engineering data when the proposed application of the component alters the technical data. The letter shall certify that the component application meets specification requirements.

3.2.2.6 Temperature Rating
All components used shall be designed to operate within the full temperature range specified. The component data sheets shall be the only accepted form of validation of the temperature range. Testing and/or screening of commercial grade components are not permitted.

3.2.3 Capacitors

The DC and AC voltage ratings as well as the dissipation factor of a capacitor shall exceed the worst-case design parameters of the circuitry by 150% except for Supercaps which shall be 110%. Supercaps are capacitors rated less than 10 working VDC with capacitance values greater than or equal to 1.0F. Capacitor encasements shall be resistant to cracking, peeling and discoloration. With the exemption of Surface Mount Capacitors, all capacitors shall be insulated and shall be marked with their capacitance values and working voltages. Electrolytic capacitors shall not be used for capacitance values of less than 1.0 µF and shall be marked with polarity.

3.2.4 Potentiometers

Potentiometers with ratings from 1 to 2 W shall meet Military Type RV4 requirements. Potentiometers with ratings less than 1 W shall be used only for trimmer type function. The potentiometer power rating shall be at least 100% greater than the maximum power requirements of the circuit.

3.2.5 Resistors

Fixed carbon film, deposited carbon, or composition-insulated resistors shall conform to the performance requirements of Military Specifications MIL-PRF-22684F and Amendment 1. All resistors shall be insulated and shall be marked, except for surface mount, with their resistance values. Resistance values shall be indicated by the EIA color codes, or stamped value. The value of the resistors shall not vary by more than 5% between -34.60°F and 165.20°F.

3.2.5.1 Thermal

Special Ventilation or Heat Sinking shall be provided for all 2 W or greater resistors. They shall be insulated from the PCB.

3.2.6 Semiconductor-Devices

3.2.6.1 Solid State

All Solid State devices, except LEDs, shall be of the silicon type.

3.2.6.2 Transistors / IC / Diodes

All Transistors, Integrated Circuits, and Diodes shall be a standard type listed by EIA. With exemption of Surface Mount Components, Transistors, Integrated Circuits and Diodes shall be clearly identifiable.

3.2.6.3 Metal Oxide Semi-Conductor

All Metal Oxide Semi-Conductor components shall contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields.

3.2.6.4 Device Pin 1

Device Pin "1" locations shall be properly marked on the PCB adjacent to the pin.

3.2.7 Transformers / Inductors
With the exemption of Surface Mount Components, all power transformers and inductors shall have the manufacturer's name or logo and part number clearly and legibly printed on the case or lamination. All transformers and inductors shall have their windings insulated, shall be protected to exclude moisture, and their leads color coded with an approved EIA color code or identified in a manner to facilitate proper installation.

### 3.2.8 Triacs

Each triac with a designed circuit load of greater than 0.5 A at 120 VAC shall be mounted to a heat sink with thermal conductive compound or material, in addition to being mechanically secured.

### 3.2.9 Circuit Breakers

Circuit Breaker shall be UL 489 approved. The trip and frame sizes shall be plainly marked (marked on the breaker by the manufacturer), and the Amperes rating shall be marked and visible from the front of the breaker. Contacts shall be silver alloy and enclosed in an arc-quenching chamber. Overload tripping shall not be influenced by an ambient air temperature range of from 0.4°F to 122 °F. The minimum Interrupting Capacity shall be 5,000 A RMS when the breaker is secondary to a UL approved fuse or primary circuit breaker and both breakers in concert provide the rated capacity. For circuit breakers 80 A and above, the minimum interrupting capacity shall be 10,000 A RMS. Circuit breakers shall be the trip-free type with medium trip delay characteristic (Carling switch Time Delay Curve #24 or equal).

### 3.2.10 Fuses

All Fuses shall be 3.15 A Glass Slow Blow type and resident in a holder. Fuse size rating shall be labeled on the chassis, PCB or beside the holder. Fuses shall be easily accessible and removable without use of tools.

### 3.2.11 Switches

#### 3.2.11.1 Dual-Inline-Package-(DIP)

Dual-inline-package, quick snap switches shall be rated for a minimum of 30,000 operations per position at 50 mA, 30 VDC. The switch contact resistance shall be 100 mΩ maximum at 2 mA, 30 VDC. The contacts shall be gold over brass (or silver). Contact for VAC or 28 VDC and shall be silver over brass (or equal). The DIP shall have recessed switches to prevent accidental switching.

#### 3.2.11.2 5 VDC Logic Switch

5 VDC Logic rating shall be 0.4VA @ 20VAC or DC with contact material of gold over nickel plating or copper alloy. The switch shall be rated for a minimum of 40,000 operations.

#### 3.2.11.3 12 -24 VDC Logic/Control Switches

12-24 VDC control switch contacts shall be rated for a minimum of 5 A resistive load at 120 VAC or 28 VDC and shall be gold over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

#### 3.2.11.4 Power Rating

The switch contacts shall be rated for a minimum of 10 A resistive load at 120 VAC or 28 VDC and shall be silver over brass or equal.

### 3.2.12 Terminal Blocks
The terminal blocks shall be barrier type, rated at 20 A and 600 VAC RMS minimum. The terminal screws shall be 0.313 in minimum length nickel plated brass binder head type with screw inserts of the same material. Screw size is called out under the associated file, panel or assembly.

3.2.13 Wiring / Cabling / Harnesses

3.2.13.1 Harnesses

Harnesses shall be neat, firm and properly bundled with external protection. They shall be tie-wrapped and routed to minimize cross talk and electrical interference. Each harness shall be of adequate length to allow any conductor to be connected properly to its associated connector or termination point. Conductors within an encased harness have no color requirements. Printed circuit motherboards are to be used where possible to eliminate or reduce cabinet wiring.

3.2.13.2 AC Wiring

Wiring containing AC shall be bundled separately or shielded separately from all DC logic voltage control circuits.

3.2.13.3 Cabling

Cabling shall be routed to prevent conductors from being in contact with metal edges. Cabling shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

3.2.13.4 Labeling

All conductors, except those which can be readily traced, shall be labeled. Labels attached to each end of the conductor shall identify the destination of the other end of the conductor.

3.2.13.5 Conforming

All conductors shall conform to MIL-W-16878G/1 or better and shall have a minimum of 19 strands of copper. The insulation shall be polyvinyl chloride with a minimum thickness of 10 mils or greater. Where insulation thickness is 15 mils or less, the conductor shall conform to MIL-W-16878/17.

3.2.13.6 Conductor Color

Conductor Color identification shall be as follows:

- **AC-** White.
- **EG** Solid green or continuous green color with 1 or more yellow stripes.
- **DC logic ground** Solid white or continuous white with a red stripe.
- **AC+** Solid black or continuous black with colored stripe.
- **DC logic ungrounded or signal** Any color not specified.
3.2.14 Indicators / Displays

All indicators and character displays shall be readily visible at a radius of up to 4 ft within the cone of visibility when the indicator is subjected to 97,000 lux (9,000 foot-candles) of white light with the light source at 45 +/-2 degrees to the front panel.

3.2.14.1 Indicators

All indicators and character displays shall have a minimum 90 degrees cone of visibility with its axis perpendicular to the panel on which the indicator is mounted. All indicators shall be self-luminous. All indicators shall have a rated life of 100,000 hours minimum. Each LED indicator shall be white or clear when off and visibly illuminated when on.

3.2.14.2 Character Displays

Liquid Crystal Displays (LCD) shall operate at temperatures of -4 °F to 158 °F.

3.2.15 Connectors

3.2.15.1 Keyed

All connectors shall be keyed to prevent improper insertion of the wrong connector. The mating connectors shall be designated as the connector number and male/female relationship, such as C1P (plug or PCB edge connector) and C1S (socket).

3.2.15.2 Plastic Circular / M Type

Each pin and socket contacts for connectors shall be beryllium copper construction sub-plated with 0.00005 in nickel and plated with 0.0000299 in gold. Pin diameter shall be 0.061811 in. Each pin and socket contact shall use the AMP Incorporated Part #601105-1 or AMP Incorporated Part #91002-1 contact insertion tool and the AMP Incorporated Part #305183 contact extraction tool.

3.2.15.3 PCB Connectors

3.2.15.3.1 PCB Edge Connectors

Each PCB Edge connector shall have bifurcated gold-plated contacts. The PCB receptacle connector shall meet or exceed the following:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Voltage</td>
<td>600 VAC RMS</td>
</tr>
<tr>
<td>Current Rating</td>
<td>5.0 A</td>
</tr>
<tr>
<td>Insulation Material</td>
<td>Diallyl Phthalate or Thermoplastic</td>
</tr>
<tr>
<td>Insulation Resistance</td>
<td>5,000 MΩ</td>
</tr>
<tr>
<td>Contact Material</td>
<td>Copper alloy plated with 0.00005 in of nickel and 0.000015 in of gold</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>0.006 Ω maximum</td>
</tr>
</tbody>
</table>

3.2.15.3.2 Two-Piece PCB Connectors

Each Two-Piece PCB connector shall meet or exceed DIN 41612.

3.2.15.4 Wire Terminal Connectors

Each wire terminal connector shall be solderless with PVC insulation and a heavy-duty short-locking spade type connector. Each terminal connector shall be crimped using a Controlled-Cycle type crimping tool.
3.2.15.5 Flat Cable Connectors

Each flat cable connector shall be designed for use with 26 AWG cable; shall have dual cantilevered phosphor bronze contacts plated with 0.00015 of gold over 0.00005 inches of nickel; and shall have a current rating of 1 A minimum and an insulation resistance of 5 MΩ minimum.

3.2.15.6 PCB Header Post Connectors

Each PCB header post shall be 0.00155 in² by 0.343 in high; shall be mounted on 0.156 in centers; and shall be tempered hard brass plated with 0.000015 in of gold over 0.00005 in of nickel.

3.2.15.7 PCB Header Socket Connectors

Each PCB header socket block shall be nylon or diallyl phthalate. Each PCB header socket contact shall be removable, but crimp-connected to its conductor. The Contractor shall list the part number of the extraction tool recommended by its manufacturer. Each PCB header socket contact shall be brass or phosphor bronze plated with 0.00010 in of gold over 0.00005 in of nickel.

3.2.15.8 Surge Protection Device

A three-electrode gas tube type that is capable of withstanding 15 pulses of peak current each of which will rise in 8 μs and fall in 20 μs to 0.5 of the peak voltage at 3-minute intervals. Peak current rating shall be 20,000 A. It shall have the following ratings:

- **Impulse Breakdown:** Less than 1,000 Volts in less than 0.1 μs at 10 kV/μs.
- **Standby Current:** Less than 1 mA.
- **Striking Voltage:** Greater than 212 V.
3.3 Mechanical

3.3.1 Assemblies

All assemblies shall be modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBs. Assemblies shall be provided with 2 guides for each plug-in PCB or associated device (except relays). The guides shall extend to within 0.75 in from the face of either the socket or connector and front edge of the assembly. If Nylon guides are used, the guides shall be securely attached to the file or assembly chassis.

3.3.2 PCB Design

No components, traces, brackets or obstructions shall be within 0.125 in of the board edge (guide edges). The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all PCBs. Devices to prevent PC Board from backing out of their assembly connectors shall be provided.

3.3.3 Model Numbers

The manufacturer's model and serial number shall appear on the rear panel of all equipment supplied (where such panel exists). In addition to any assignment of model numbers by the manufacturer, the model number identified in this standard shall be displayed on the front panel in bold type, at least 0.25 in high.

3.3.4 PCB Connectors

All PCB Connectors mounted on a motherboard shall be mechanically secured to the chassis or frame of the unit or assembly.

3.3.5 Fasteners

All screw type Fasteners shall utilize locking devices or locking compounds except for finger screws, which shall be captive.

3.3.6 Workmanship

Workmanship shall conform to the requirements of this specification and be in accordance with the highest industry standards.

3.3.7 Tolerances

The following tolerances shall apply, except as specifically shown on the plans or in these specifications:

<table>
<thead>
<tr>
<th>Material</th>
<th>Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Metal</td>
<td>+/- 0.0525 in</td>
</tr>
<tr>
<td>PCB</td>
<td>+/- 0.010 in</td>
</tr>
<tr>
<td>Edge Guides</td>
<td>+/- 0.015 in</td>
</tr>
</tbody>
</table>
3.4 Engineering

3.4.1 Human Engineering

3.4.1.1 Equipment

The Equipment shall be engineered for simplicity, ease of operation and maintenance.

3.4.1.2 Knobs

Knobs shall be a minimum of 0.5 in diameter and a minimum separation of 0.5 in edge to edge.

3.4.1.3 PCB

PCBs shall slide smoothly in their guides while being inserted into or removed from the frame and shall fit snugly into the plug-in PCB connectors. PCBs shall require a force no less than 4.5 lbs or greater than 50 lbs for insertion or removal.

3.4.2 Design Engineering

The design shall be inherently temperature compensated to prevent abnormal operation. The circuit design shall include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range. The design shall take into consideration the protection of personnel from all dangerous voltages.

3.4.3 Generated Noise

No item, component or subassembly shall emit a noise level exceeding the peak level of 55 dBA when measured at a distance of one meter away from its surface, except as otherwise noted. No item, component or subassembly shall emit a noise level sufficient to interfere with processing and communication functions of the controller circuits.
3.5 Printed Circuit Boards

3.5.1 Design, Fabrication and Mounting

The Design, Fabrication and Mounting of components and assemblies shall comply with the Association Connecting Electronics Industries (IPC) Standards as specifically listed in this standard. In the event of any conflict between the requirements of this standard and IPC standards, the IPC Standards shall govern.

3.5.1.1 Contacts on PCBs

All contacts on PCBs shall be plated with a minimum thickness of 0.00003 in gold over a minimum thickness of 0.000075 in nickel.

3.5.1.2 PCB Design

PCB design shall be such that when a component is removed and replaced, no damage is done to the board, other components, conductive traces or tracks.

3.5.1.3 Fabrication

Fabrication of PCBs shall be in compliance with IPC-4101B and Amendment 2, except as follows:

3.5.1.3.1 Copper Tracks

NEMA FR-4 glass cloth base epoxy resin copper clad laminates 0.0625 in minimum thickness shall be used. Inter-component wiring shall be by laminated copper clad track having a minimum weight of 1.0 ounces per square foot with adequate cross section for current to be carried. All copper tracks shall be plated or covered by solder mask to provide complete coverage of all exposed copper tracks. Jumper wires to external PCB components shall be from plated-through padded holes and as short as possible.

3.5.1.3.2 Pits, Dents, Bows and Twists

Grade of Pits and Dents shall be of Grade B or better. The permissible bow or twist shall be Class C or better.

3.5.1.4 Mounting

The mounting of parts and assemblies on the PCB shall conform to IPC-2221A, Class 3, except as follows:

3.5.1.4.1 Semiconductor Devices

Semiconductor devices that dissipate more than 250 mW or cause a temperature rise of 50 °F or more shall be mounted with spacers, transipads or heat sinks where applicable to prevent contact with the PCB.

3.5.1.4.2 Residual Flux

When completed, all residual flux shall be removed from the PCB.
3.5.1.4.3 Resistance

Except where Surface Mount Components are used, the resistance between any 2 isolated, independent conductor paths shall be at least 100 MΩ when a 500 VDC potential is applied.

3.5.1.4.4 Coated

All PCBs shall be conformal coated with a UV Tracer. This coating shall conform to the configuration of the object coated, applied on the completed board assembly. The coating shall be resistant to the effect of moisture and solvents.

3.5.1.4.5 Lateral Separation

Where less than 0.125 in lateral separation is provided between the PCB (or the components of a PCB) and any metal surface, a 0.03125 in ± 0.0156 in thick Mylar (polyester) plastic cover shall be provided on the metal to protect the PCB.

3.5.1.5 Connector Edges

Each PCB connector edge shall be chamfered at 30 degrees from board side planes. The key slots shall also be chamfered so that the connector keys are not extracted upon removal of board or jammed upon insertion. The key slots shall be 0.045 in ± 0.005 in for 0.1 in spacing and 0.055 in ± 0.005 in for 0.156 in spacing.

3.5.2 Soldering

3.5.2.1 Hand Soldering

Hand soldering shall comply with IPC-J-STD-00D and Amendments.

3.5.2.2 Automatic Flow Soldering

Automatic flow soldering shall be a constant speed, conveyor system with the conveyor speed set at optimum to minimize solder peaks or points. Temperature shall be controlled to within ± 46.4 °F of the optimum temperature. The soldering process shall result in the complete coverage of all copper runs, joints and terminals with solder except that which is covered by an electroplating process. Wherever clinching is not used, a method of holding the components in the proper position for the flow process shall be provided.

3.5.2.3 Time-Temperature

If exposure to the temperature bath is of such time-temperature duration, as to come within 80% of any component's maximum specified time-temperature exposure, that component shall be hand soldered to the PCB after the flow process has been completed.

3.5.3 Definitions

Definitions for the purpose of this section on PCBs shall be taken from IPC-613 and Amendment 1.
3.6 Quality Control

3.6.1 Components

All components shall be lot sampled to assure a consistent high conformance standard to the design specification of the equipment.

3.6.2 Subassembly, Unit or Module

Complete electrical, environmental and timing compliance testing shall be performed on each module, unit, printed circuit or subassembly. Housing, chassis, and connection terminals shall be inspected for mechanical sturdiness, and harnessing to sockets shall be electrically tested for proper wiring sequence. The equipment shall be visually and physically inspected to assure proper placement, mounting, and compatibility of subassemblies.

3.6.3 Predelivery Repair

3.6.3.1 Defects / Deficiencies

Any defects or deficiencies found by the inspection system involving mechanical structure or wiring shall be returned through the manufacturing process or special repair process for correction.

3.6.3.2 PCB Flow Soldering

PCB flow soldering is allowed a second time if copper runs and joints are not satisfactorily coated on the first run. Under no circumstances shall a PCB be flow soldered more than twice.

3.6.3.3 Hand Soldering

Hand soldering is allowed for printed circuit repair.
3.7 Electrical, Environmental and Testing Requirements

3.7.1 General

The requirements called out in these specifications dealing with equipment evaluation are a minimum guide and shall not limit the testing and inspection to insure compliance.

3.7.2 Certification

These test procedures shall be followed by the Contractors who shall certify that they have conducted inspection and testing in accordance with these specifications.

3.7.3 Inspection

A visual and physical inspection shall include mechanical, dimensional and assembly conformance of all parts of these specifications.

3.7.4 Environmental and Electrical

All components shall properly operate within the following limits unless otherwise noted:

- **Applied Line Voltage**: 90 to 135 VAC, note “Power Failure / Restoration” limits
  - Frequency: 60 (+/-3.0) Hz
  - Humidity: 5% to 95%
  - Ambient Temperature: -34.6°F to +165.2°F

3.7.4.1 Commencement Operation

All circuits, unless otherwise noted, shall commence operation at or below 90 VAC as the applied voltage is raised from 50 to 90 VAC at a rate of 2 (+/-0.5) V / s.

3.7.4.2 Equipment Compliance

All equipment shall be unaffected by transient voltages normally experienced on commercial power lines. Where applicable, equipment purchased separately from a cabinet (which normally is resident) will be tested for compliance to this standard.

3.7.4.3 Power Line Surge Protection

The power line surge protection shall enable the equipment being tested to withstand (non-destructive) and operate normally following the discharge of a 25 μF capacitor charged to ±2,000 V, applied directly across the incoming AC line at a rate of once every 10 s for a maximum of 50 occurrences per test. The unit under test will be operated at 68°F ±41°F and at 120 (+/-12) VAC.

3.7.4.4 Operating

The equipment shall withstand (nondestructive) and operate normally when one discharge pulse of plus or minus 300 V is synchronously added to its incoming AC power line and moved uniformly over the full wave across 360 degrees or stay at any point of Line Cycle once every second. Peak noise power shall be 5 kW with a pulse rise time of 500 ns. The unit under test will be operated at 68°F ±41°F and at 120 (+/-12) VAC.
3.7.4.5 Modules

The controller unit communications modules shall be tested resident in an ATC 2070 controller unit.

3.7.4.6 UL Requirements

Equipment shall comply only with the requirements of UL Bulletin of Research No. 23, "Rain Tests of Electrical Equipment."

3.7.4.7 Normal Operation

All equipment shall continue normal operation when subjected to the following:

3.7.4.7.1 Low Temperature Test

With the item functioning at a line voltage over Electrical Range the Device in its intended operation, the ambient temperature shall be lowered from 68 °F to 34.6 °F at a rate of not more than 64.4 °F per hour. The item shall be cycled at -34.6 °F for a minimum of 5 hours and then returned to 68 °F at the same rate.

3.7.4.7.2 High Temperature Test

With the item functioning at a line voltage over Electrical Range the Device in its intended operation, the ambient temperature shall be raised from 68 °F to 165.2 °F at a rate of not more than 64.4 °F per hour. The item shall be cycled at 165.2 °F for 5 hours and then returned to 68 °F at the same rate. The test shall be repeated with the line voltage at 135 VAC.

3.7.4.7.3 Normal Operation

All equipment shall resume normal operation following a period of at least 5 hours at -34.6 °F and less than 10 percent humidity and at least 5 hours at 165.2 °F and 22% humidity, when 90 VAC is applied to the incoming AC.

3.7.4.8 Humidity and Ambient Temperature

The relative humidity and ambient temperature values in the following table shall not be exceeded.

<table>
<thead>
<tr>
<th>Ambient Temperature/ Dry Bulb (in °F)</th>
<th>Relative Humidity (in percent)</th>
<th>Ambient Temperature/ Wet Bulb (in °F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-34.6 to 33.98</td>
<td>10</td>
<td>1.04 to 108.86</td>
</tr>
<tr>
<td>33.98 to 114.8</td>
<td>95</td>
<td>108.86</td>
</tr>
<tr>
<td>119.84</td>
<td>70</td>
<td>108.86</td>
</tr>
<tr>
<td>129.92</td>
<td>50</td>
<td>108.86</td>
</tr>
<tr>
<td>140.0</td>
<td>38</td>
<td>108.86</td>
</tr>
<tr>
<td>149.72</td>
<td>28</td>
<td>108.86</td>
</tr>
<tr>
<td>160.16</td>
<td>21</td>
<td>108.86</td>
</tr>
<tr>
<td>165.2</td>
<td>18</td>
<td>108.86</td>
</tr>
</tbody>
</table>

3.7.4.9 Opening and Closing of Contacts

All equipment shall be capable of normal operation following opening and closing of contacts in series with the applied voltage at a rate of 30 openings and closings per minute for a period of 2 minutes in duration.
3.7.5 Contractor’s Testing Certification

3.7.5.1 QC / Final Test

A complete QC / final test report shall be supplied with each item. The test report shall indicate the name of the tester and shall be signed by a responsible manager.

3.7.5.2 Quality Control Procedure & Test Report

The quality control procedure and test report format shall be supplied to the Engineer for approval within 15 days following the award of the contract. The quality control procedure shall include the following:

- Acceptance testing of all supplied components.
- Physical and functional testing of all modules and items.
- A minimum 100-hour burn-in of all equipment.
- Physical and functional testing of all items.
3.8 General Controller Unit

3.8.1 Controller Unit Composition

The Controller Unit shall be composed of the Unit Chassis, modules and assemblies per their version. The following is a list of 2070 Versions, their interface rolls and composition:

<table>
<thead>
<tr>
<th>UNIT VERSION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>2070E UNIT</td>
<td>LITE Unit mates to the 170 &amp; ITS Cabinets. It consists of: UNIT CHASSIS, 2070-1E CPU, 2070-2A (2B if ITS Cabinet), FI/O, 2070-3B FRONT PANEL and 2070-4 POWER SUPPLY</td>
</tr>
</tbody>
</table>

Note: See Section 3.17 for NEMA compatible versions if the ATC 2070.

3.8.2 Communications and Option Modules

The communications and option modules shall be called out separately from the unit version. The composition weight shall not exceed 25 lbs.

3.8.3 Chassis

The Chassis top and Bottom, Internal Structure Supports, Back Plane Mounting Surface, Module Plates, Power Supply Enclosure, and Front Panel shall be made of minimum aluminum sheet. The Chassis Side panels shall be 0.090 inches minimum sheet.

3.8.4 Power Failure Power Restoration Operations

It is noted that the Power Failure Power Restoration operations of this unit are specific to the requirements of the user. All associated modules shall comply to said operations.

3.8.5 2070 Unit Module

2070 UNIT module / assembly power limitations shall be as follows:

<table>
<thead>
<tr>
<th>Models</th>
<th>+5VDC</th>
<th>+12VDC iso</th>
<th>+12VDC ser</th>
<th>-12 VDC ser</th>
</tr>
</thead>
<tbody>
<tr>
<td>2070-1E CPU</td>
<td>1.0 A</td>
<td>250 mA</td>
<td>-----</td>
<td>-----</td>
</tr>
<tr>
<td>2070-2A FI/O</td>
<td>250 mA</td>
<td>750 mA</td>
<td>-----</td>
<td>-----</td>
</tr>
<tr>
<td>2070-2B FI/O</td>
<td>250 mA</td>
<td>500 mA</td>
<td>-----</td>
<td>-----</td>
</tr>
<tr>
<td>2070-3A,B&amp;D FPA</td>
<td>500 mA</td>
<td>-----</td>
<td>50 mA</td>
<td>50 mA</td>
</tr>
<tr>
<td>2070-3C FPA</td>
<td>500 mA</td>
<td>-----</td>
<td>50 mA</td>
<td>50 mA</td>
</tr>
<tr>
<td>2070-5 VME Cage</td>
<td>5.0 A</td>
<td>-----</td>
<td>200 mA</td>
<td>200 mA</td>
</tr>
<tr>
<td>2070-6A &amp; Others</td>
<td>900 mA</td>
<td>-----</td>
<td>300 mA</td>
<td>300 mA</td>
</tr>
<tr>
<td>2070-7 All Comm</td>
<td>250 mA</td>
<td>-----</td>
<td>50 mA</td>
<td>50 mA</td>
</tr>
</tbody>
</table>

3.8.6 EIA-485 Communications Links
All circuitry associated with the EIA-485 Communications links shall be capable of reliably passing a minimum of 1.0 Mbps. Isolation circuitry shall be by optical isolator technologies.

3.8.7 EIA-485 Line Drivers/Receivers

The EIA-485 Line Drivers/Receivers shall be socket mounted or surface mounted and shall not draw more than 35 mA in active state and 20 mA in inactive state. A 100 Ω Termination Resistor shall be provided across each Differential Line Receiver Input. The MOTHERBOARD's control signals (e.g., SP1-RS) shall be active, or asserted, when the positive terminal (e.g., SP1-RS+) is a lower voltage than its corresponding negative terminal (e.g., SP1-RS-). A control signal is inactive when its positive terminal voltage is higher than its negative terminal. Receive and transmit data signals shall be read as a "1" when the positive terminal's (e.g., SP1-TXD+) voltage is higher than its corresponding negative terminal (e.g., SP1-TXD-). A data value is "0" when its positive terminal's (e.g., SP1-TXD+) voltage is lower than its negative terminal (e.g., SP1-TXD-).

3.8.8 Sockets

Sockets for devices (called out to be socket mounted) shall be "xx" pin AUGAT 500/800 series AG10DPC or equal.

3.8.9 Frame Address

SP5 and SP3 SDLC frame address assignments (Command/Response) are as follows:

<table>
<thead>
<tr>
<th></th>
<th>SP 5</th>
<th>SP3</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU 2070-1</td>
<td>&quot;19&quot;</td>
<td>&quot;19&quot;</td>
</tr>
<tr>
<td>FI/O 2070-2A</td>
<td>&quot;20&quot;</td>
<td>&quot;NA&quot;</td>
</tr>
<tr>
<td>Manufacturer Use</td>
<td>128-254</td>
<td>128-254</td>
</tr>
<tr>
<td>CPU Broadcast to all</td>
<td>&quot;255&quot;</td>
<td>&quot;255&quot;</td>
</tr>
</tbody>
</table>

All other addresses are reserved or assigned by the Agency with the exception of NEMA TS 2 Type 1 Requirements (see Sections 3.17 and 3.18). The SDLC response shall contain the frame address of the Command sender.
3.9 Model 2070-1 CPU Module

3.9.1 Model 2070-1E CPU Module

The Model 2070-1E CPU Module shall be a single board module meeting the 2X WIDE Board requirements. The module shall be furnished normally resident in the Motherboard Slot A5. The module shall meet all the requirements listed under this section and Appendix A Section Details. The Model 2070-1E Module shall use a Freescale MC68EN360 CPU or equal (references to MC68EN360 will refer to either), clocked at 24.576 MHz minimum.

3.9.1.1 Dual SCC Device

A Dual SCC Device (asynch / synch) and associated circuitry shall be furnished to provide two additional system serial ports. The Dual SCC1 shall be assigned to the System Serial Port SP1 meeting all requirements called out for SP1 except where noted. The Dual SCC2 shall be assigned as System Serial Port SP8. The SP8 and associated circuitry shall interface with the MC68EN360 address and data structure and serially be connected to the external world via the DB 25 Pin C13S Connector located on the module front panel. The SP8 shall meet all SP2 Port requirements except where noted, including EIA 485 drivers / receivers and synchronous data rate of 153.3 kbps.

3.9.1.2 MC68EN360 SCC1

The MC68EN360 SCC1 shall be reassigned to Ethernet (ENET) Network meeting Ethernet 10 Mbps IEEE 802.3 (TP) 10 BASE T Standard Requirements, both hardware and software. The CPU network lines shall be connected to a port on the Network Switch. Four LEDs labeled “10/100 and Link/Act” shall be mounted on the front panel signifying Ethernet operational conditions between the CPU and the Network Switch.

3.9.1.3 Module 2070-1E Power Requirements

The 2070-1E CPU Module shall not draw more than 1.00 A of +5VDC & 250 mA of ISO+12 VDC.

3.9.1.4 The C13S Connector

The C13S Connector shall be a DB25S connector and shall be located on the Module 2070-1X CPU front panel and shall contain signals for SP8, LINESYNC, NRESET, POWERDOWN, and an isolated BIAS +5VDC as specified in the following subsections and as listed in A9-7. TX and RX LEDs shall be provided as shown in Figure A-7 Model 2070-1E CPU Modules & Serial Port/SDLC Protocol.

3.9.1.4.1 Serial Port SP8

System Serial Port 8 (SP8) shall be isolated, converted to EIA-485, and then routed to Connector C13S. SP8 shall meet all SP2 Port requirements except where noted.

3.9.1.4.2 LINESYNC and POWERDOWN

LINESYNC and POWERDOWN lines shall each be isolated, converted to EIA-485, and then routed to connector C13S for external module use.

3.9.1.4.3 NRESET

CPU_Reset and POWER UP lines shall be isolated, then OR’d to form NRESET. NRESET shall then be converted to EIA-485 and routed to connector C13S for external module use.
3.9.1.5 Contiguous Addresses

A block of 16 MB contiguous address space for each specified memory (DRAM, SRAM and FLASH) shall be allocated on an even boundary. The SRAM and FLASH memories shall be accessed through the OS-9 Supplied File Manager.

3.9.1.6 Incoming +5 VDC

When the incoming +5 VDC falls below its operating level, the SRAM shall drop to its standby state and the SRAM and TOD Clock shall shift to the +5 VDC Standby Power. An on-board circuit shall sense the +5 VDC Standby Power and shift to an On-board CPU Power Source. When the incoming +5 VDC rises to within its operating level, the appropriate circuitry shall shift from standby power to incoming +5 VDC.

3.9.1.7 RAM Memory

A minimum of 8 MB of DRAM memory, organized in 32-bit words, shall be provided. A minimum of 512 kB of SRAM will be available for agency use, organized in 16 or 32-bit words shall be provided. The time from the presentation of valid RAM address, select lines, and data lines to the RAM device to the acceptance of data by the RAM device shall not exceed 80 ns and shall be less as required to fulfill zero wait state RAM device write access under all operational conditions.

3.9.1.8 Flash Memory

A minimum of 8 MB of FLASH memory, organized in 16- or 32-bit words, shall be provided. The 2070-1E shall be equipped with all necessary circuitry for writing to the FLASH memory under program control. No more than 2 MB of FLASH Memory shall be used for the Boot Image and a minimum of 6 MB shall be available for Agency use. A maximum of 2 MB of Flash Memory shall be reserved the Boot Image only. Flash memory shall have a minimum rated capacity of 100,000 read/write cycles and be industrial grade or better.

3.9.1.9 Time-of-Day Clock

A software settable hardware Time-of-Day (TOD) clock shall be provided. It shall, under on-board standby power maintain an accuracy of ±1 minute per 30 days at 25°C. The clock shall provide a minimum fractional second resolution of 10 ms and shall track seconds, minutes, and hours, day of month, month, and year.

3.9.1.10 CPU_Reset

A software-driven CPU_Reset signal (Active LOW) shall be provided to reset other controller systems. The signal output shall be a driver capable of sinking 30 mA at 30 VDC. Execution of the program module “cpureset” in the boot image shall assert the CPU_Reset signal once. CPU_Reset shall be executed when the controller starts up or is rebooted using the OS-9 break command.

3.9.1.11 CPU_ACTIVE LED Indicator

An open-collector output, capable of sinking 30 mA at 30 VDC, shall be provided to drive the Front Panel Assembly CPU_ACTIVE LED Indicator. The LED shall default to ON when the controller starts up.

3.9.1.12 Tick Timer

The OS-9 Tick Timer interrupt shall be derived from the each transition of LINESYNC signal, with a tick rate of 120 ticks per second.
3.9.1.13 SRAM and TOD Clock

The SRAM and TOD Clock Circuitry under Standby mode shall draw no more than 8 µA at 2.5 VDC and 35 °C. An On board Capacitor supply shall hold up SRAM and TOD for a minimum of 7 days.

3.9.1.14 Network Switch, Model 2070-1E

The Model 2070-1E CPU Module shall be provided with an integrated Store-and-Forward Network Switch per the IEEE 802.3, 802.3u and 802.3 x specifications. The switch shall be configured with two ports connected to the front panel RJ-45 connectors (C14S) and a third port shall be connected to the CPU. A fourth Port on the Network Switch shall be used to route Ethernet across the Motherboard to the “A” Connector’s Network Lines. DC Grounding around the network connectors and lines shall be provided. The Network Lines shall be assigned as: NetP5 TX+, TX-, RX+ and RX- respectively.

3.9.2 Datakey

A Datakey Keyceptacle™ (KC4210, KC4210PCB or equal) shall be mounted on the CPU module front panel. Power shall not be applied to the receptacle if the key is not present.

The contractor shall supply an 8 Mb Memory Size Datakey (SFK8Mb or equal) with each MODEL 1E CPU module unless specified otherwise. The Datakey shall be temperature rated for –40 °C to +85 °C (–40°F to 185 °F) operation, shall be blue in color, and shall be initialized to the format and default values defined below. External capability to program the CPU Datakey shall be provided by the contractor.

When programmed, the memory on the key of header shall be organized as follows:

<table>
<thead>
<tr>
<th>Bytes</th>
<th>Description</th>
<th>Default Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-2</td>
<td>16 bit Frame Check Sequence (FCS) calculated as defined in clause 4.6.2 of ISO/IEC 3309. This FCS is calculated across bytes 3-64</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Key Type</td>
<td>See table below</td>
</tr>
<tr>
<td>4</td>
<td>Header Version</td>
<td>2</td>
</tr>
<tr>
<td>5-8</td>
<td>Latitude</td>
<td>0.0</td>
</tr>
<tr>
<td>9-12</td>
<td>Longitude</td>
<td>0.0</td>
</tr>
<tr>
<td>13-14</td>
<td>Controller ID</td>
<td>0xFFFF</td>
</tr>
<tr>
<td>15-16</td>
<td>Communication drop number</td>
<td>0xFFFF</td>
</tr>
<tr>
<td>17-20</td>
<td>IP Address</td>
<td>10.20.70.51</td>
</tr>
<tr>
<td>21-24</td>
<td>Subnet Mask</td>
<td>255.255.255.0</td>
</tr>
<tr>
<td>25-28</td>
<td>Default Gateway</td>
<td>10.20.70.254</td>
</tr>
<tr>
<td>29</td>
<td>Startup Override</td>
<td>0xFF</td>
</tr>
<tr>
<td>30-64</td>
<td>Reserved for Agency use</td>
<td>All bytes set to 0xFF</td>
</tr>
<tr>
<td>65 to End</td>
<td>User Data</td>
<td>All bytes set to 0xFF</td>
</tr>
</tbody>
</table>

When programmed, Byte 3 of the header shall contain the Key Type value as defined in the following table:

<table>
<thead>
<tr>
<th>Key Type</th>
<th>Model No.</th>
<th>Memory Size</th>
<th>Sector Size</th>
<th>Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>DK1000</td>
<td>1 kb</td>
<td>2 B</td>
<td>611-0006-002A</td>
</tr>
<tr>
<td>2.</td>
<td>LCK16000</td>
<td>16 kb</td>
<td>2 B</td>
<td>611-0070-008A</td>
</tr>
<tr>
<td>3.</td>
<td>SFK2Mb</td>
<td>2 Mb</td>
<td>64 kB</td>
<td>611-0089-004A</td>
</tr>
<tr>
<td>4.</td>
<td>SFK4Mb</td>
<td>4 Mb</td>
<td>64 kB</td>
<td>611-0104-002A</td>
</tr>
<tr>
<td>5.</td>
<td>SFK8Mb</td>
<td>8 Mb</td>
<td>64 kB</td>
<td>611-0132-006A</td>
</tr>
<tr>
<td>6.</td>
<td>SFK32Mb</td>
<td>32 Mb</td>
<td>64 kB</td>
<td>611-0164-005A</td>
</tr>
</tbody>
</table>
The data format in the CPU Datakey header for the Latitude and Longitude fields shall comply with IEEE/ANSI 754-1985 STD. All the other fields shall follow a Big Endian Format.

The Startup Override byte, not the Key Type, may be used to override the default controller startup procedure, as described in Section 3.9.3.3.3 Startup Procedure.

3.9.3 Model 2070-1E CPU Module Software

The following shall be supplied:
- Operating System
- Drivers and Descriptors
- Application Kernel
- Deliverables
- Error Handler

3.9.3.1 Operating System

The CPU Module shall be supplied with Microware Embedded OS-9 Release 1.3 or later with kernel edition #376 or later. The following modules shall be included:

1. Embedded OS-9 Real Time Kernel
2. Sequential Character File Manager (SCF)
3. Stacked Protocol File Manager (SPF)
4. Pipe File Manager (PIPEMAN)
5. Random Block File Manager (RBF)
6. C Shared Library (CSL)

Boot Image shall include the following utility modules:

<table>
<thead>
<tr>
<th>Break</th>
<th>Date</th>
<th>Deiniz</th>
<th>Devs</th>
<th>Free</th>
<th>Copy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dir</td>
<td>Tmode</td>
<td>Edt</td>
<td>List</td>
<td>Load</td>
<td>Deldir</td>
</tr>
<tr>
<td>Dump</td>
<td>Del</td>
<td>Ident</td>
<td>Iniz</td>
<td>Irqs</td>
<td>Events</td>
</tr>
<tr>
<td>Echo</td>
<td>Format</td>
<td>Dcheck</td>
<td>Login</td>
<td>Link</td>
<td>Kermit</td>
</tr>
<tr>
<td>Tsmon</td>
<td>Mdir</td>
<td>Mfree</td>
<td>Pd</td>
<td>Makdir</td>
<td>Save</td>
</tr>
<tr>
<td>Attr</td>
<td>Rename</td>
<td>Procs</td>
<td>Unlink</td>
<td>Sleep</td>
<td>Xmode</td>
</tr>
<tr>
<td>Shell</td>
<td>Build</td>
<td>Setime</td>
<td>Merge</td>
<td>Grep</td>
<td></td>
</tr>
<tr>
<td>Tee</td>
<td>Printnv</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The Boot Image with the above utilities and including the network driver and descriptor shall be loaded into RAM as part of OS-9 initialization as defined in Section 3.9.3.3.2 Hardware Initialization.

3.9.3.2 Drivers and Descriptors

3.9.3.2.1 Supplied Modules

Supplied modules shall be re-entrant, address independent, and shall not contain self-modifying code.

Device drivers which require extensions to the standard OS-9 libraries shall use the _os_getstat() and _os_setstat() functions.

A custom setstat code and parameter structure are defined as follows:

```c
#define SS_2070 0x2070
```
error_code _os_getstat(path_id path, SS_2070, PB2070 *pb);
error_code _os_setstat(path_id path, SS_2070, PB2070 *pb);

typedef struct
{
    u_int32 code;
    u_int32 param1;

    union
    {
        u_int32 param;
        void  *pointer;
    }
    param2;
} PB2070, *pb;

The following subcodes for use with PB2070.code are also defined:

#define GS2070_Status 0x1C
#define SS2070_SSig 0x1A
#define SS2070_IFC 0x22
#define SS2070_OFC 0x23
#define SS2070_Timer_Null 0x0000 (Default State)
#define SS2070_Timer_Sig 0x1000
#define SS2070_Timer_Cyc 0x1001
#define SS2070_Timer_Start 0x1002
#define SS2070_Timer_Stop 0x1003
#define SS2070_Timer_Reset 0x1004

Note: When PB2070.param2.pointer is used, PB2070.param1 should be loaded with the size of what
PB2070.param2.pointer is referencing. When calling _os_getstat() or _os_setstat(), all reserved or
unused parameters and fields in PB2070 should be loaded with 0 (zero).

3.9.3.2.2 Memory Drivers

Drivers shall be provided to access the FLASH, SRAM, and DRAM memories. The following descriptors
shall apply:

/f0FLASH drive non-volatile, writeable
/ddFLASH drive OS-9 default device for /f0
/f0wpFLASH Drive as /f0 except write protected
/f0fmtFLASH Drive as /f0 except format enabled
/r0SRAM Drive non-volatile ramdisk
/r0fmtSRAM Drive as /r0 except format enabled
/r2DRAM Drive volatile 2 MB ramdisk, not automatically initialized

3.9.3.2.3 MC68360 Internal Timers

A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided. Timer
resolution shall be one count equals 100 μs and all timer periods shall be specified in units of hundreds of
microseconds (μs).

A signal of "0" shall be an invalid signal and the driver shall return an E$PARAM error if received.

Access to the MC68EN360 internal timers shall be through the descriptors as listed under Descriptor.
The timers should be set to the SS2070_Timer_Null Mode upon initialization.

3.9.3.2.3.1 Descriptor

Descriptor names for each timer:

- timer1 = access to MC68EN360's internal timer #1
- timer2 = access to MC68EN360's internal timer #2
- timer3 = access to MC68EN360's internal timer #3
- timer4 = access to MC68EN360's internal timer #4
- timer12 = access to MC68EN360's internal timer #1 & #2 [cascaded]
- timer34 = access to MC68EN360's internal timer #3 & #4 [cascaded]

3.9.3.2.3.2 Timer Standard

Timer Standard OS-9 Function Calls:

- error_code _os_open (char *timer_desc_name, path_id *path);
- error_code _os_read (path_id path, void *timer_value, u_int32 *size);
  Note: Prior to calling _os_read(), size must be loaded with the value 4 and timer value must be pointed to a u_int32. _os_read() shall read the current timer value and load it into timer_value as µs x 100.
- error_code _os_close (path_id path);

3.9.3.2.3.3 Time Extension

Timer Extension to Standard OS-9 Function Calls:

The timer drivers shall support the following modes using the following function with the SS_2070 option code and a custom parameter block structure:

- error_code _os_setstat(path_id path, SS_2070, PB2070 *pb);

a. Send signal after specified time interval. Sets timer to zero and schedules individual one-shot signal. After one-shot signal is sent, timer shall stop (SS2070_Timer_Stop).

  pb→ code = SS2070_Timer_Sig; /* request for one-shot signal */
  pb→ param1= signal;
  pb→ param2.param = period;

b. Send recurring periodic signal. Sets timer to zero and schedules repeating periodic signal.

  pb→ code = SS2070_Timer_Cyc (0x1001); /* request for periodic signal */
  pb→ param1 = signal;
  pb→ param2.param = period;

c. Start timer. Starts the timer if stopped or null. Timer will free run in a periodic mode, starting at the current timer value as its initial value and timer’s maximum allowable time as its timer period. Timer will not send a signal and any pending signals will be cancelled.

  pb→ code = SS2070_Timer_Start; /* start timer if stopped */

c. Reset timer. Stops timer if running, resets timer value to zero, and cancels any pending signals.

\[
\text{pb\rightarrow code} = \text{SS2070_Timer_Reset}; \quad /* \text{reset timer (stop and zero)} */
\]

3.9.3.2.3.4 Timer Extension

Timer Extension to Standard OS-9 Function Calls:

The timer driver shall support the following function with the SS_2070 option code and custom parameter block structure:

\[
\text{error\_code \_os\_getstat(path\_id path, SS\_2070, PB2070 *pb)};
\]

a. Retrieve current timer configuration.

\[
\text{typedef struct}
\]

\[
\{
\quad \text{u\_int32 value;}
\quad \text{u\_int32 mode;}
\quad \text{u\_int32 signal;}
\quad \text{u\_int32 period;}
\}\ \text{Timer\_status;}
\]

\[
\text{pb\rightarrow code} = \text{GS2070\_Status} \ (0x1C) \quad /* \text{Request timer status data} */
\]

\[
\text{pb\rightarrow param1} = \text{sizeof(Timer\_status)}
\]

\[
\text{pb\rightarrow param2\_pointer} = \&\text{Timer\_status}
\]

Status data shall be returned in the structure pointed to by \text{pb\rightarrow param2\_pointer} as follows:

\[
\text{pb\rightarrow param2\_pointer\rightarrow value} \quad /* \text{current timer value in } \mu\text{s} \times 100 */
\]

\[
\text{pb\rightarrow param2\_pointer\rightarrow mode} \quad /* \text{SS2070\_Timer\_Sig if one-shot signal pending, SS2070\_Timer\_Cyc if periodic signal pending, SS2070\_Timer\_Start if free running, SS2070\_Timer\_Stop if not active, SS2070\_Timer\_Reset if timer is reset, SS2070\_Timer\_Null when timer is first initialized} */
\]

\[
\text{pb\rightarrow param2\_pointer\rightarrow signal} \quad /* \text{signal code pending if SS2070\_Timer\_Sig or SS2070\_Timer\_Cyc, 0 otherwise} */
\]

\[
\text{pb\rightarrow param2\_pointer\rightarrow period} \quad /* \text{timer period in } \mu\text{s} \times 100 \text{ if SS2070\_Timer\_Sig or SS2070\_Timer\_Cyc and Maximum Timer Period if SS2070\_Timer\_Start, 0 otherwise} */
\]
The following values shall be returned when the timer is in the SS2070_Timer_Null (Timer initialized) Mode:

```
Timer Mode = SS2070_Timer_Null
Timer Value = 0
Timer Period = 0
Timer Signal = 0
```

The following values shall be returned when the timer is in the SS2070_Timer_Start Mode:

```
Timer Mode = SS2070_Timer_Start
Timer Value = Running Timer Value
Timer Period = Maximum Timer Period
Timer Signal = 0
```

The following values shall be returned when the timer is in the SS2070_Timer_Stop Mode:

```
Timer Mode = SS2070_Timer_Stop
Timer Value = Current Timer Value
Timer Period = 0
Timer Signal = 0
```

The following values shall be returned when the timer is in the SS2070_Timer_Reset Mode:

```
Timer Mode = SS2070_Timer_Reset
Timer Value = 0
Timer Period = 0
Timer Signal = 0
```

### 3.9.3.2.3.5 Timer Period

All timer periods are specified in units of hundreds of μs (e.g. a timer period of 7 = 700 μs). The minimum allowed timer period shall be 500 μs. The maximum timer period for timers 1-4 shall be 6.5535 s. The maximum timer period for timer12 and timer34 shall be 429496.7295 s. The driver shall return error E$Param from _os_setstat() if the requested timer period is outside the allowable range.

### 3.9.3.2.4 CPU Datakey

Access and control to the CPU Datakey shall be provided through the following descriptor name and OS-9 functions:

- **Descriptor name:**
  - `datakey` = access to the CPU Datakey

- **Function Calls:**
  - `error_code = _os_open (char *datakey_desc_name, path_id *path);`
  - `error_code = _os_close (path_id path);`
  - `error_code = _os_read (path_id path, void *data_buffer, u_int32 *data_size);`
  - `error_code = _os_write (path_id path, void *control, u_int32 *data_size);`
  - `error_code = _os_seek(path_id path, u_int32 *position); /* sets read / write offset */`
error_code = _os_ss_erase(path_id path, u_int32 num_sec_erase);
/* erases sector(s) if pointer is on a block boundary, returns E$PARAM error if not on a boundary */

error_code = _os_gs_pos(path_id path, u_int32 *position);
/* gets current file pointer position */

error_code = _os_gs_size(path_id path, u_int32 *size);
/* gets current datakey size */

Error codes returned by Function calls:

E$NotRdy if datakey is not inserted
E$Seek if Offset plus *data_size is beyond end of CPU Datakey.
E$EOF if upon read or write, the last byte of CPU Datakey has previously been processed.
Note: Use of SCF to implement the datakey driver is not allowed.

3.9.3.2.5 Flow Control Modes

The asynchronous serial communications device drivers shall support the six flow control modes (FCM#) described below:

<table>
<thead>
<tr>
<th>FCM#</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.</td>
<td>No Flow Control Mode: The driver transmits data regardless of the state of CTS. Upon a write command, the driver asserts RTS, and de-asserts RTS when data transmission is completed. This is the default mode. When user programs issue the first RTS related command, the driver switches to Manual Flow Control Mode (FCM# 1).</td>
</tr>
<tr>
<td>1.</td>
<td>Manual Flow Control Mode: The driver transmits data regardless of the state of CTS. The user program has absolute control of the RTS state. The driver doesn’t automatically assert or de-assert RTS.</td>
</tr>
<tr>
<td>2.</td>
<td>Auto-CTS Flow Control Mode: The driver transmits data only when CTS is externally asserted. The user program has absolute control of the RTS state. The driver doesn’t automatically assert or de-assert RTS.</td>
</tr>
<tr>
<td>3.</td>
<td>Auto-RTS Flow Control Mode: The driver transmits data regardless of the state of CTS. Upon a write command, the driver asserts RTS, and de-asserts RTS when data transmission is completed and any configured RTS extension is elapsed. If the user program asserts RTS, then RTS remains on until the user program de-asserts RTS. If the user program de-asserts RTS before the transmission buffer is empty, the driver holds RTS on until the transmission buffer is empty and any configured RTS extension is elapsed.</td>
</tr>
<tr>
<td>4.</td>
<td>Fully Automatic Flow Control Mode: The driver transmits data only when CTS is externally asserted. Upon a write command, the driver asserts RTS and waits for CTS, starts data transmission when CTS is asserted, and de-asserts RTS when data transmission is completed and any configured RTS extension is elapsed. If user program asserts RTS, then RTS remains on until the user program de-asserts RTS. If the user program de-asserts RTS before the transmission buffer is empty, the driver holds RTS on until the transmission buffer is empty and any configured RTS extension is elapsed.</td>
</tr>
</tbody>
</table>
| 5.   | Dynamic Flow Control Mode: The driver transmits data only when CTS is externally asserted. The driver controls RTS based on the status of its receiving buffer. The
driver asserts RTS continuously as long as its receiving buffer has sufficient capacity to store incoming data. If the receiving buffer approaches full, the driver de-asserts RTS until enough data has been read from the buffer to create sufficient receive capacity.

3.9.3.2.5.1 Serial Device Driver

The serial device driver shall be able to set user options via _os_setstat() and return status via _os_getstat(). To support legacy application programs, the device driver shall also be able to set user options via _os_ss_size() and to return status via _os_gs_size():

```
error_code_os_setstat(path_id path, SS_2070, void *pb);
error_code_os_getstat(path_id path, SS_2070, void *pb);
error_code_os_ss_size(path_id path, u_int32 size);
error_code_os_gs_size(path_id path, u_int32 *size);
```

Note: The preferred method of accessing serial device drivers is through _os_setstat() and _os_getstat(). The _os_ss_size() and _os_gs_size() interface may not be required by future versions of this specification and is therefore not recommended for new development.

The option subcodes to be passed in pb→code and the data to be contained in pb→param1 are defined as follows. pb→param2 is unused here and should be set to 0 (zero). For _os_ss_size() and _os_gs_size(), the size argument is the same format as pb→param1.

3.9.3.2.5.2 Supported Setstat

The supported_os_setstat() / _os_ss_size() options shall be as follows.

a. Subcode passed in pb→code is SS2070_OFC (0x23).

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24</td>
<td>Auto RTS turn-off extension in number of characters (range:0-255, 0=default).</td>
</tr>
<tr>
<td>23-14</td>
<td>Reserved for future use.</td>
</tr>
<tr>
<td>13</td>
<td>Inhibit return of error E$Write from _os_write() when transmit buffer full in FCM# 2, 4, 5 (default=0, 0=error, 1=block)</td>
</tr>
<tr>
<td>12</td>
<td>Inhibit variable SCC MRBLR (default =0; 0=NO; 1=inhibit).</td>
</tr>
<tr>
<td>11</td>
<td>Inhibit SCC TODR (default=0; 0=NO; 1=inhibit).</td>
</tr>
<tr>
<td>10-8</td>
<td>Flow Control Mode Number (FCM#) (range:0-5).</td>
</tr>
<tr>
<td>7-0</td>
<td>Subcode SS2070_OFC (0x23).</td>
</tr>
</tbody>
</table>

Variable MRBLR (MC68EN360 SCC)

To reduce the IRQ handler overhead, the MC68EN360 SCC driver shall use variable MRBLR as follows. If SS2070_OFC bit 12 is set to 1, the MRBLR shall be fixed at 16 for all baud rates. Variable MRBLR is not required for SP1 or SP8 on the 2070-1E CPU Module.

<table>
<thead>
<tr>
<th>Baud Rate</th>
<th>MRBLR Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>1200</td>
<td>1</td>
</tr>
<tr>
<td>2400</td>
<td>2</td>
</tr>
<tr>
<td>4800</td>
<td>4</td>
</tr>
<tr>
<td>9600</td>
<td>8</td>
</tr>
<tr>
<td>19200 &amp; Higher</td>
<td>16</td>
</tr>
</tbody>
</table>

TODR (68360 SCC)
TODR requests processing a new TX buffer immediately. To reduce impact on other serial channel operations, SS2070_OFC bit 11 may be set to 1 to prevent assertion of TODR. TODR is not required for SP1 or SP8 on the 2070-1E CPU Module.

b. Subcode passed in pb→code is SS2070_IFC (0x22).
   Data passed in pb→param1 is defined as follows:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-11</td>
<td>Reserved for Future Use.</td>
</tr>
<tr>
<td>10</td>
<td>DCD must be asserted to receive data (default=0; 0=NO; 1=YES).</td>
</tr>
<tr>
<td>9-8</td>
<td>Reserved for Future Use.</td>
</tr>
<tr>
<td>7-0</td>
<td>Subcode = SS2070_IFC (0x22).</td>
</tr>
</tbody>
</table>

c. Subcode passed in pb→code is SS2070_SSig (0x1A).

1. If CTS is currently negated and bits 16-31 are not all 0:
   Setting the SS2070_SSig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal as soon as CTS is asserted.
   Setting the SS2070_SSig parameter block bit 12 (send when CTS is negated) will cause the controller to send a one-shot signal immediately.

2. If CTS is currently asserted and bits 16-31 are not all 0:
   Setting the SS2070_SSig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal immediately.
   Setting the SS2070_SSig parameter block bit 12 (send when CTS is negated) will cause the controller to send a one-shot as soon as CTS is negated.

3. If both bits 11 and 12 of the SS2070_SSig parameter block are set, and bits 16-31 are not all 0:
   The controller will send a one-shot signal upon the next change of CTS state

Data passed in pb→param1 is defined as follows:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>A signal number to be sent to calling process when the state of an input changes.</td>
</tr>
<tr>
<td>15-13</td>
<td>Reserved for Future Use.</td>
</tr>
<tr>
<td>12</td>
<td>Send signal when CTS is de-asserted.</td>
</tr>
<tr>
<td>11</td>
<td>Send signal when CTS is asserted.</td>
</tr>
<tr>
<td>10-8</td>
<td>Reserved for Future Use.</td>
</tr>
<tr>
<td>7-0</td>
<td>Subcode = SS2070_SSig (0x1A).</td>
</tr>
</tbody>
</table>

3.9.32.5.3 Supported Getstat

The supported _os_getstat() / _os_gs_size() options shall be as follows.

a. Subcode passed in pb→code is GS2070_Status (0x1C).
   Data returned in pb→param1 is defined as follows:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>Current unfilled transmit buffer character count of the serial device driver.</td>
</tr>
<tr>
<td>15-11</td>
<td>Reserved for Future Use.</td>
</tr>
<tr>
<td>10-8</td>
<td>Current Flow Control Mode Number (FCM#).</td>
</tr>
</tbody>
</table>
### 3.9.3.2.6 Device Drivers Compliant

Device drivers compliant with the OS-9 SCFMAN shall be provided for CPU Activity LED Indicator and DST time correction features. The descriptor names shall be as follows:

- `led` = access to CPU Activity LED Indicator
- `dstclock` = access to DST Clock correction

The standard OS-9 SCFMAN library calls and their functions are as follows:

```c
error_code _os_open (char *desc_name, path_id *path);
/* open descriptor for command */

error_code _os_close (path_id path);
/* close descriptor */

error_code _os_write (path_id path, void *value, u_int32 *data_size);
/* set value of function */

*value = 1, turn on LED or enable DST correction (default)

*value = 0, turn off LED or disable DST correction set u_int32*data_size to 1

error_code _os_read (path_id path, void *value, u_int32 *data_size);
/* get current state set u_int32*data_size to 1 */
```

### 3.9.3.2.7 Manufacturer Support

The manufacturer shall provide the following features to support the TOD operation and synchronization.

#### 3.9.3.2.7.1 Leap Year and Daylight Savings Time

Leap Year and DST Adjustments - The OS-9 System clock / calendar shall automatically be adjusted to account for DST and leap years.

#### 3.9.3.2.7.2 Setting Hardware Clock

Setting Hardware Clock from OS-9 System Clock - A device driver compatible with the OS-9 SCFMAN shall be provided to allow the hardware TOD clock/calendar to be updated from the OS-9 system clock under application control. The descriptor name shall be “ClockUpdate.” Opening the descriptor shall cause the driver to synchronize the clock to a minimum of 10 ms resolution. The driver shall compensate for any time elapsed during the process of updating the hardware clock.

#### 3.9.3.2.7.3 Setting OS-9 System Clock

<table>
<thead>
<tr>
<th>7</th>
<th>Reserved for Future Use.</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>Overrun error –0=no error; 1=error has occur since last GS2070_Status call.</td>
</tr>
<tr>
<td>5</td>
<td>Frame error –0=no error; 1=error has occur since last GS2070_Status call.</td>
</tr>
<tr>
<td>4</td>
<td>Parity error –0=no error; 1=error has occur since last GS2070_Status call.</td>
</tr>
<tr>
<td>3</td>
<td>Reserved for Future Use.</td>
</tr>
<tr>
<td>1</td>
<td>DCD state –0=de-asserted; 1=asserted.</td>
</tr>
<tr>
<td>0</td>
<td>CTS state –0=de-asserted; 1=asserted.</td>
</tr>
</tbody>
</table>
Setting OS-9 System Clock from Hardware Clock - At system power up, the OS-9 system TOD clock/calendar shall automatically be updated from the hardware TOD clock. The clocks shall be synchronized to a minimum of 10 ms resolution.

3.9.3.2.8 Flash Ram Drive

The FLASH drive shall be protected from corruption. It shall be protected using the Write Protect (WP) bit of the Base Register. When writing to the FLASH drive the current sector of FLASH being written shall first be backed up in SRAM. The backup sector copy shall be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy.

A user write operation shall restore the valid backup sector copy first. Execution of the program module, “FLRESTORE,” in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay. “FLRESTORE” shall accept a delay parameter in seconds ranging from 0 to 600 seconds. The default delay factor is 30 seconds.

3.9.3.3 OS-9 Application Kernel

3.9.3.3.1 Boot Sysreset

The provided software shall boot OS-9 from SYSRESET. The entire program shall be resident in FLASH Memory. The serial port descriptors shall be configured with the default parameters as listed in A9-16.

3.9.3.3.2 Hardware Initialization

Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test), and forking OP_EXEC shall be completed in less than 4 seconds. This startup time shall be measured from the release of SYSRESET to the turn on of the CPU_ACTIVE LED using a user level program named ONLED. The ONLED program shall be the last module loaded into RAM and executed using opeexec or a startup file.

3.9.3.3.3 Startup Procedure

The boot image init module shall be configured with the default directory name as /f0wp and sysgo as the first executable module.

Sysgo shall operate as follows:

1. Sysgo shall set the execution directory to /f0wp/CMDS
2. Sysgo shall check if the backspace key (0x08) is being received on /sp4 (c50j). If received, Sysgo shall:
   a. Fork a shell with no arguments on /sp4 using the current directory.
   b. Remain an active process and monitor the shell for termination. If the shell does terminate, Sysgo shall fork another shell with no arguments on /sp4. Unless Sysgo dies, a shell shall always be provided on /sp4.
3. If the backspace key was not received, Sysgo shall check for the presence of a Datakey. If present and valid (Datakey Header Version 2 or greater), Sysgo shall check the Startup Override Byte in the Datakey header.

If Startup Override is 0x01, Sysgo shall:
a. Fork a shell that executes a shell script stored on the Datakey in the following format. Immediately following the key header shall be the size of the script in bytes. The script shall immediately follow the size value, and shall be stored as ASCII text.

b. If there is any error reading or starting the script or if the shell terminates with an error, Sysgo shall display an error message on /sp4 and fork another shell as described in step 2. If there are no errors executing the script, Sysgo shall exit without forking another shell.

If Startup Override is 0x02, Sysgo shall:
   a. Fork an executable module stored on the Datakey immediately following the header.
   b. If there is any error loading or forking the module, Sysgo shall display an error message on /sp4 and fork a shell as described in step 2. If there are no errors forking the module, Sysgo shall then exit without forking a shell.

4. If the backspace key was not received and Startup Override Byte is 0xFF:
   a. Sysgo shall fork the module named /f0wp/OPEXEC if present at /f0wp.
   b. If there is any error loading or forking OPEXEC, Sysgo shall display an error message on /sp4 and fork a shell as described in step 2. If there are no errors forking OPEXEC, Sysgo shall then exit without forking a shell.

5. If the backspace key was not received, Startup Override Byte is 0xFF, and there is no OPEXEC file:
   a. Sysgo shall fork a shell that executes a shell script named /f0wp/startup if present at /f0wp.
   b. If there is any error reading or starting the script or if the shell terminates with an error, Sysgo shall display an error message on /sp4 and fork another shell as described in step 2. If there are no errors executing the script, Sysgo shall exit without forking another shell.

6. If the backspace key was not received, Startup Override Byte is 0xFF, and there is no OPEXEC and no startup file:
   a. Sysgo shall fork a shell as described in step 2.

3.9.3.3.4 Short Out

A Short Out is defined as the period of time between ACFAIL/POWER DOWN transition to LOW and back to HIGH without a SYSRESET transition to LOW. ACFAIL/POWER DOWN transitions shall generate an interrupt. The interrupt shall update an OS-9 event named "ACFAIL". The "ACFAIL" event shall set a value 1 indicating an ACFAIL condition occurred for the DOWN transition and set 0 indicating non-ACFAIL condition for the HIGH transition. The IRQ7 and auto-vector 31(7) shall not be used to update the "ACFAIL" event.

In addition, the ACFAIL condition shall generate the OS-9 auto-vector 30(6) interrupt service. Each interrupt service installed shall exit with the "Carry Bit" set allow OS9 to propagate the ACFAIL interrupt. The Contractor shall supply an interrupt handler at priority 255 that acknowledges and clears the interrupt.

Priority 1 shall be reserved for the OS-9 system.
3.9.3.3.5 Long Out

A Long Out is defined as ACFAIL transition to LOW followed by a SYSRESET going LOW. The SYSRESET going HIGH shall be followed by an operating system reboot.

3.9.3.4 Error Handler

3.9.3.5 Initialization and Power-Up Test

A manufacturer may include an error handling routine to save troubleshooting data regarding initialization, power-up test abnormalities and other error conditions. If used, the error report shall be stored in the file /r0/ErrorReport and shall not exceed 11kb in size.

3.9.3.6 Network Requirements

On the MODEL 2070-1E CPU module, an OS-9 SPF Ethernet hardware driver and descriptor for the 68360 (SCC1) shall be provided in the operating system Boot Image. The descriptor shall be named spqe0.

3.9.3.6.1 BOOTOBJS

The following OS-9 modules should be included in the /f0/CMDS/BOOTOBJS flash disk directory to allow for standard TCP/IP network communications using Ethernet Protocol over Ethernet hardware and/or Serial Line Internet Protocol (SLIP) or Point-to-Point Protocol over serial links:

1. Drivers and Descriptors for PPP.
2. Drivers and Descriptors for SLIP.
3. LAN Comm Pak modules: spenet, enet, spip, ip0, sptcp, tcp0, spudp, udp0, spraw, raw0, sproute, route0, spipcp, ipcp0, spip0, spudp, udp0, splip, spip, spip0, spslip, sps10
4. Network modules pkman, pkdvr, pk, pks
5. Network Trap Handler: netdb_local, netdb_dns
6. NFS Modules: nfs, nfsnul and nfs_devices.

The PPP and SLIP descriptors shall have baud rates and ports set as follows and be stored in the /f0/CMDS/BOOTOBJS directory,

- hdlic0 and sps10 configured to use /sp1 and 38400 bps
- hdlic1 and sps11 configured to use /sp2 and 115200 bps
- hdlic2 and sps12 configured to use /sp3 and 115200 bps
- hdlic3 and sps13 configured to use /sp4 and 38400 bps

3.9.3.6.2 CMDS

The following Network utilities shall be included and shall reside in the /f0/CMDS directory as identified in this specification.

- arp, dhcp, ftp, ftpd, ftpdc, idbdump, idbgen, rpcdbgen, ifconfig, inetd, ipstart, ndbmod, netstat, ping, route, routed, telnet, telnetdc, hostname, nfsc, mount, rpcdump, nfsstat, exportfs, portmap, ppd, chat, pppauth, nfsd, mountd, and showmount.

3.9.3.6.3 Multi-user Functionality
The boot image init module shall be configured with a “default directory name” as /f0wp. This will allow login and tsmon to provide the user with login prompt from the terminal port or from the network via a telnet session.

The following OS-9 modules should be included in the operating system boot image for the implementation of multi-user mode.

   login, tsmon

3.9.3.6.4 Network Configuration

The modules inetdb, inetdb2 and rpcdb shall be generated by the make utility via the use of a makefile and the network configuration files residing the /f0/ETC directory. The generated inetdb, inetdb2 and rpcdb modules should be re-located to the /f0/CMDS/BOOTOBJS directory where they will be pick-up by the network configuration shell scripts located at /f0/SYS. The modules shall be configured with the network default values as defined in Section 3.9.2 Datakey via the interfaces.conf shell script.

3.9.3.6.5 Netcfg

A Utility Program named netcfg shall be provided that reads the CPU Datakey for an IP Address, Subnet Mask and Default Gateway. If the Datakey is present and valid (Datakey Header Version 2 or greater), netcfg shall set the IP Address, Subnet Mask and Default Gateway of the Model 2070 Controller when executed by a user at the command line. The netcfg utility shall create a new inetdb, inetdb2 and rpcdb database module based on the Datakey network parameters or network parameters from the command line. The new inetdb, inetdb2 and rpcdb modules should be re-located to the /f0/CMDS/BOOTOBJS directory where they will be pick-up by the network configuration shell scripts located at /f0/SYS. The netcfg shall also allow the user to read, write and display network parameters to and from the Datakey via the command line prompt. If the Datakey is not present or invalid and the flag option is not “n” netcfg shall display an error and exit without altering the network configuration. The netcfg utility shall reside in /f0/CMDS.

Netcfg options:

   a= Write IP Address in Datakey
   m= Write Netmask Address in Datakey
   g= Write Gateway Address in Datakey

If the checksum is incorrect when executing the –a, -m or –g option the following will occur:

   1. The default Datakey data will be loaded.
   2. The networking changes will be made to the default networking parameters.
   3. The CRC will be recalculated.
   4. The networking parameters will be written to the Datakey.

This option loads default networking parameters into the Datakey.

   -d= Write Default Networking Parameters in the Datakey

This option will display the networking information contained in the Datakey.

   -i= Reads Networking Parameters from the Datakey

This option will set the networking parameters permanently on the controller using values from the Datakey.
-c= Changes interfaces.conf and builds inetdb, inetdb2 and rpcdb.

Normal operation of this option will be:

1. Read the Datakey networking parameters
2. Delete interfaces.conf and routes.conf from /f0/etc
3. Write new interfaces.conf and routes.conf in /f0/etc.
4. Execute idbgen to create new inetdb and inetdb2
5. Executes rpcdbgen to create a new rpcdb
6. Delete inetdb, inetdb2 and rpcdb in /f0/cmds/bootobjs.
7. Relocate inetdb, inetdb2 and rpcdb in /f0/cmds/bootobjs.

This option will display the current Controller Network Parameters such as the IP Address, Netmask, Gateway and MAC Address. This requires the network Stack to be initialized.

-r= Reads current Networking Configuration.

This option will set the networking parameters dynamically on the controller using values from the Datakey

-s= Sets Network Configuration Dynamically from the Datakey.

This option will set the networking parameters permanently on the controller using values from the command line. The option will do the same functions as option "c" with network parameters from the command line.

-n= Set Controller Network Parameters without the Datakey

The netcfg -n -a [opts] -m [opts] -g [opts] shall allow the user to permanently set the IP Address, Subnet Mask and Gateway of the Model 2070 Controller when executed by the user at the command line using parameters provided by the user at the command line.

Where opts may be IP Address in the format xxx.xxx.xxx.xxx, netmask in the format xxx.xxx.xxx.xxx and gateway as xxx.xxx.xxx.xxx.

Example, the following sets the IP Address, Netmask and Gateway permanently in the Model 2070 Controller to 10.20.70.51, 255.255.255.0 and 10.20.70.254:

netcfg -n -a 10.20.70.51 –m 255.255.255.0 – g 10.20.70.254

These options will display the help menu on how to use the netcfg utility.

h, ?, blank = displays the help menu

The help menu shall consist of the following:

Netcfg Usage:

netcfg [- a ] [-m ] [-g ] [-n ] [-d ] [- i ] [-r ] [ - s ]
-a follows Ip Address ; Write IP Address in Datakey
-m follows Netmask ; Write Netmask Address in Datakey
-g follows Gateway ; Write Gateway Address in Datakey
-d  ;Write Default Networking Parameters in the Datakey
-i  ;Reads Networking Parameters from the Datakey
-c  ;Changes interfaces.conf and builds inetdb, inetdb2 and rpcdb.
-r  ;Reads current Controller Networking Configuration.
-s  ;Sets Network Configuration Dynamically from the Datakey.

-n <network parameters> ;Set Controller Network Parameters without Datakey

Example of option –n:
netcfg -n –a 10.20.70.51 –m 255.255.255.0 –g 10.20.70.254

See Section 3.9.2 for additional information.

3.9.3.6.6  ETC

A set of example configuration files consistent with the above networking modules shall be provided in the
/f0/ETC directory. This directory shall contain the following text files:
hosts, hosts.equiv, networks, protocols, services, inetd.conf, resolv.conf, hosts.conf, rpc, interfaces.conf,
routes.conf, makefile, nfs.map, nfsd.map

3.9.3.7  Standard Microware File System Configuration

3.9.3.7.1  Directories

The Model 2070 shall follow Standard Microware File System Configuration. A /f0/CMDS,
/f0/CMDS/BOOTOBJS, /f0/ETC and /f0/SYS directories shall be implemented. Execute permission shall
be included in the attributes of files in the /f0/CMDS directory. Sysgo should set its execution directory to
/f0wp/CMDS prior to spawning opexec or other processes. The /f0/CMDS/BOOTOBJS shall contain the
modules as identified above and other customizable descriptors and modules. The /f0/SYS shall also
contain the following four standard OS-9 network configuration shell script files: startspf, startnfs, loadspf
and loadnfs.

3.9.3.7.2  Password

The /f0/SYS shall contain a "password" file. The password file should follow Microware's password file
format for the addition and configuration of multiuser functionality and password protection. A user name
"super" with password as "user" shall be defined in the password file.

A Termcap text file shall be include in the /f0/SYS directory. This Termcap file shall contain description
fields defining the capability names and values of the front panel DISPLAY.

3.9.3.7.3  Utilities

The utilities tar, make, fixmod, mshell and vi shall be included in the /f0/CMDS directory.

3.9.3.7.4  Ver

A Ver utility shall be provided as part of the OS-9 Image and shall allow access to Controller's
Manufacturer Name, Image Build Number, TEES Version or ATC 2070 Standard Version, Image Build
Date and CPU Module Type. Ver should display the contents of a data module named "bootid" which contains in its data area the following structure:

```c
/* bootid_body*/
struct bootid_body {
    char *mfgname; /* Manufacturer Name */
    char *cpumoduletype; /* CPU Module Type */
    char *teesrelease; /* TEES Version or ATC 2070 Standard Version */
    char *imagebuilddate; /* Image Build Date */
    u_int16 majv; /* Major Version */
    u_int16 minv; /* Minor Version */
    u_int16 sv1; /* Sub-Version 1 */
    u_int16 sv2; /* Sub-Version 2 */
    u_int16 sv3; /* Sub-Version 3 */
    u_int16 dv; /* Development Version */
};
```

OS-9 editmod shall be used to generate the header file and the "bootid" module using the following config.des file:

```c
#include "defines.h" /*this file contains customization for the module */
#include <module.des> /* required for module definitions in modhcom */

/* this is the bootid module structure */
struct bootid_body
{
    pointer u_int32 mfgname = mn, "Manufacturer Name";
    pointer u_int32 cpumoduletype = cmt, "CPU Module Type";
    pointer u_int32 teesrelease = tr, "TEES Release";
    pointer u_int32 imagebuilddate = ibd, "Image Build Date";
    u_int16 majv, "Major Version";
    u_int16 minv, "Minor Version";
    u_int16 sv1, "Sub-Version 1";
    u_int16 sv2, "Sub-Version 2";
    u_int16 sv3, "Sub-Version 3";
    u_int16 dv, "Development Version";
}, "bootid_body";
```

string mn = MfgName;
string cmt = CPUModuleType;
string tr = TEESRelease;
string ibd = ImageBuildDate;
string mod_name = "bootid";

init bootid_body
{
    majv = MajorVer;
    minv = MinorVer;
    sv1 = SubVer1;
    sv2 = SubVer2;
    sv3 = SubVer3;
};

init modhcom
When run via the command line the Ver utility shall display the following:

Ver options:
  -a  Shows all information
  -b  CPU Module Type
  -d  Image Build Date
  -m  Controller’s Manufacturer Name
  -t  TEES Version
  -v  Image Build Version Number
  -?  Display Help

CPU Type shall display 2070-1E.
Image Build Date shall be in the form of mm/dd/yyyy
Manufacturer’s name shall be shown as one word only.
The TEES version shall be of the form “TEES XXXX EY” where XXXX is the year of the TEES and Y is any Errata if applicable. The ATC 2070 Standard version shall be of the form “ATC2070 XXXX” where XXXX is the version (e.g. “ATC2070 0300” refers to ATC 2070 Standard v03.00”). Ver without an option shall be the same as Ver -a.

Ver –a shall display all information as shown by the following example:

2070-1E
03/06/2008
Vendor Name
TEES 2008 E5 ; E5 Would be blank if there are no Errata.
Build 2.7.3.0.0.0

The help menu shall consist of the following:

Ver Usage:

  -a  Shows all information
  -b  CPU Module Type
  -d  Image Build Date
  -m  Controller’s Manufacturer Name
  -t  TEES Release
  -v  Image Build Version Number
  -?  Display Help
3.9.4 Re-Flash Utility

A Utility Program shall be provided that would allow the user to upgrade (re-flash) the Boot Image for the Model 2070-1E CPU as defined in Section 3.9.3 Module 2070-1E CPU Module Software. This utility shall provide the capabilities for upgrading the Operating System and drivers when available by the manufacturer. The Utility Program shall provide the capability for the user to dynamically upgrade the Boot Image via the command prompt. The contractor shall also provide a copy in CD-ROM Memory of all files originally stored in the flash drive /f0 so that they can be reloaded as needed.

3.9.5 Communications Loading Test

The Model 2070 Controller using the Model 2070-1E CPU shall pass a Communications Loading Test consisting of Serial and Network Communications. The test shall run Sp1, Sp2, Sp3, and Sp8 at 9600 bytes per second in a continuous full duplex asynchronous/synchronous communications loop with the network stack initialized and a telnet session established for each port with standard out, in and standard error directed to the telnet session port. The test shall not exceed a maximum CPU load of 30% during test duration of 96 hours for Model 2070-1E Module.

3.9.6 Diagnostic Acceptance Test (DAT)

The standard Caltrans DAT Program shall be provided resident in the 2070 Unit as the application program.

3.9.7 Purchasing Agency

Source and object software shall be provided to the Purchasing Agency on both document listing and CD-ROM Memory. It shall provide user descriptions of test logic and reports. The Agency shall possess non-exclusive rights to this program suite.

3.9.8 Deliverables

3.9.8.1 Copies Delivery

Two copies of the following items will be provided to the purchasing Agency on a CD disk readable by a PC compatible computer.

1. Specific hardware memory addresses, including FLASH, SRAM, and DRAM starting addresses, shall be specified and provided. Written documentation of addresses shall be in PDF form and will have the file name of “Memory Map.pdf”
2. Copies of the vendor kernel, platform drivers and OS-9 utility executable modules.
3. Copy of all provided written manuals in PDF form.
4. RE-FLASH Utility and the procedures for its use in PDF form. The PDF documentation of the procedures shall have the file name of “Reflash Utility Procedures.pdf”.
3.10 Model 2070-2 Field I/O Module (FI/O)

3.10.1 Model 2070-2A Module

The Model 2070-2A Model shall consist of the Field Controller Unit; Parallel Input/Output Ports; other Module Circuit Functions (includes muzzle jumper); Serial Communication Circuitry; Module Connectors C1S, C11S, and C12S mounted on the module front plate; VDC Power Supply (+12VDC to +5VDC); and required software.

3.10.2 Model 2070-2B Module

The Model 2070-2B Model shall consist of the Serial Communication Circuitry, DC Power Supply, and Module Connector C12S mounted on the module front plate only.

3.10.3 Field I/O Controller Unit (FCU)

The FCU shall include a programmable microprocessor/controller unit together with all required clocking and support circuitry. The FCU shall be provided with in-circuit re-programmability via a JTAG or BDM port.

3.10.4 Parallel Ports

3.10.4.1 Parallel Input Ports

The Parallel Input Ports shall provide 64 bits of input using ground-true logic. Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 µA or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to the isolated +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground. The pull-up resistance shall not be less than 10K or more than 50 kΩ.

3.10.4.2 Parallel Output Ports

The Parallel Output Ports shall provide 64 bits of output. Each output written as a logic "1" shall have a voltage at its field connector output of less than 4.0 VDC. Each output written as a logic "0" shall provide an open circuit (1 Mega Ohm or more) at its field connector output. Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 mA minimum. Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 µs when connected to a load of 100 kΩ minimum. Each output circuit shall be protected from transients of 10 ±2 µs duration, ±300 VDC from a 1 kΩ source, with a maximum rate of 1 pulse per second.

3.10.4.3 Output Operation

Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing. The state of all output circuits at the time of POWER UP or in Power Down state shall be open. It shall be possible to simultaneously assert all outputs within 100 µs of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

3.10.5 Other Module Circuit Functions
3.10.5.1 Maximum Capacitive Load

A maximum capacitive load of 100 pF shall be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.

3.10.5.2 External WDT “Enable” Shunt/Toggle Switch

An External WDT “Enable” Shunt/Toggle Switch shall be provided on the board. With the jumper IN and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output 39 (Monitor Watchdog Timer Input) every 100 ms for 10 seconds or due to Set Output Command. When the shunt is missing, the feature shall not apply. This feature is required to operate with the Model 210 Monitor Unit only.

3.10.5.3 Watchdog Circuit

An FCU Watchdog Circuit shall be provided. It shall be enabled by the Field I/O firmware at Power Up with a value of 100 ms. Its enabled state shall be machine readable and reported in the FI/O status byte. Once enabled, the watchdog timer shall not be disabled without resetting the FI/O. Failure of the FI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.

3.10.5.4 One KHz Reference

A synchronizable 1 KHz time reference shall be provided. It shall maintain a frequency accuracy of ±0.01% (±0.1 counts per second).

3.10.5.5 32 Bit Millisecond Counter

A 32-bit Millisecond Counter (MC) shall be provided for “time stamping.” Each 1 kHz reference interrupt shall increment the MC.

3.10.5.6 Power Up

At Power Up, the FCU loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the “E” Bit.

3.10.5.7 Logic Switch

A LOGIC Switch shall be provided resident on the module board. The switch shall function to disconnect Serial Port 3 (SP3) from the external world, Connector C12S. Its purpose is to prevent multiple use of SP3. An LED shall be provided on the module front panel labeled “SP3 ON”. If LED light is ON, SP3 is active and available at C12S.

3.10.6 Serial Communications/Logic Circuitry

3.10.6.1 System Serial Port 5 (SP5) EIA 485 Signal

System Serial Port 5 (SP5) EIA 485 signal Lines shall enter the Field I/O Module and be split into two multi-drop isolated ports. One shall be routed to the FCU and the other converted to EIA 485, then routed to Connector C12S.

3.10.6.2 System Serial Port 3 (SP3) EIA 485 Signal

System Serial Port 3 (SP3) EIA 485 signal lines shall enter the Field I/O Module and be isolated, converted back to EIA 485 and then routed to Connector C12S.
3.10.6.3 Linesync and Power Down Lines

Linesync and Power Down Lines shall be split and isolated, one routed to FCU for shut down functions and the other changed to EIA 485; then routed to connector 12S for external module use.

3.10.6.4 CPU_Reset and Power Up

CPU_Reset and Power Up (SysReset) Lines shall be isolated and “OR’d” to form NReset. NReset shall be used to reset the FCU and other module devices. NReset shall also, be converted to EIA 485, and then routed to Connector C12S.

3.10.6.5 Module 2070-2B

If the module is 2070-2B, routing to FCU doesn’t apply.

3.10.6.6 Internal Isolation

Isolation between internal +5DC / DCG#1 and +12 DC ISO/DCG#2 and +12 DC ISO shall be used for board power and external logic.

3.10.7 Buffers

A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries. The Transition Buffer shall default to empty. There shall be two entry types: Transition and Rollover. The inputs shall be monitored for state transition. At each transition (if the input has been configured to report transition), a transition entry shall be added to the Transition Buffer. The MC shall be monitored for rollover. At each rollover transition (0xFFFF – 0x0000), a rollover entry shall be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the CPU Module upon command. Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer.

3.10.8 I/O Functions

3.10.8.1 Inputs

Input scanning shall begin at I0 (bit 0) and proceed to the highest input I63, in increasing input number. Each complete input scan shall finish within 100 $\mu$s. Once sampled, the Logic State of input shall be held until the next input scan. Each input shall be sampled 1,000 times per second. The time interval between samples shall be 1 ms ±100 $\mu$s. If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer. If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing number. The MC shall be sampled within 10 $\mu$s of the completion of the input scan.

3.10.8.2 Data Filtering

If configured, the inputs shall be filtered by the FCU to remove signal bounce. The filtered input signals shall then be monitored for changes as noted. The filtering parameters for each input shall consist of Ignore Input Flag and the On and Off filter samples. If the Ignore Input flag is set, no input transitions shall be recorded. The On and Off filter samples shall determine the number of consecutive samples an input must be on and off, respectively, before a change of state is recognized. If the change of state is shorter than the specified value, the change of state shall be ignored. The On and Off filter values shall be in the range of 0 to 255. A filter value of 0, for either or both values, shall result in no filtering for this input. The default values for input signals after reset shall be as follows:
Filtering
On and off filter values shall be set to
Transition monitoring

Enabled
5
Disabled (Timestamps are not logged)

3.10.8.3 Outputs

Simultaneous assertion of all outputs shall occur within 100 µs. Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC. The condition of the outputs shall only be "ON" if the I/O continues to receive active communications from the CPU Module. If there is no valid communications with the CPU Module for 2.0 s, all outputs shall revert to the OFF condition, and the Module Status Byte shall be updated to reflect the loss of communication from the CPU Module.

3.10.8.4 Standard Function

Each output shall be controlled by the data and control bits in the CPU Module Field I/O frame protocol as follows:

<table>
<thead>
<tr>
<th>Case</th>
<th>Output Data Bit</th>
<th>Output Control Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0</td>
<td>0</td>
<td>Output in the OFF state</td>
</tr>
<tr>
<td>B</td>
<td>1</td>
<td>1</td>
<td>Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.</td>
</tr>
<tr>
<td>C</td>
<td>0</td>
<td>1</td>
<td>Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF</td>
</tr>
<tr>
<td>D</td>
<td>1</td>
<td>0</td>
<td>Output is in the ON state.</td>
</tr>
</tbody>
</table>

3.10.8.4.1 Case A

In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured. For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 µs after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle. In Case D above, the corresponding output shall be turned ON if previously OFF and, if previously ON, remain ON until otherwise configured. All outputs shall neither glitch nor change state unless configured to do so.

3.10.8.5 Interrupts

All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts. MILLISECOND Interrupt shall be activated by the 1 kHz reference once per ms. A timestamp rollover flag set by MC rollover shall be cleared only on command. LINESYNC Interrupt - both the 0-1 and 1-0 transitions of the LINESYNC signal shall generate this interrupt. The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 kHz source for 0.5 seconds (≥60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 kHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer (≥500 consecutive millisecond interrupts).
3.10.8.6 Communication Service Routine

A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults. The communication server shall automatically:

**For Transmission:**
- Generate the opening and closing flags
- Generate the CRC value
- Generate the abort sequence (minimum of 8 consecutive ‘1’ bits) when commanded by the FCU
- Provide zero bit insertion

**For Receiving:**
- Detect the opening and closing flags
- Provide address comparison, generating an interrupt for messages addressed to the Field I/O Module, and ignoring messages not addressed to the Field I/O Module
- Strip out inserted zeros
- Calculate the CRC value, compare it to the received value, and generate an interrupt on an error
- Generate an interrupt if an abort sequence is received

3.10.8.7 Communication Processing

This task shall be to process the command messages received from the CPU Module, prepare, and start the response transmission. The response message transmission shall begin within 4 ms of the receipt of the received message. Message type processing time constraints shall not exceed 70 ms per message.

3.10.8.8 Input Processing

This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

3.10.9 Data Communication Protocols

3.10.9.1 Communications Protocol

Protocol - All communications between the CPU Module and the Field I/O shall be SDLC-compatible command-response, support 0 bit stuffing, and operate at a data rate of 614.4 kbps. The CPU Module shall always initiate the communications and if the command frame is incomplete or there is an error, no Field I/O response shall be transmitted. The number of bytes of a command or response is dependent upon the Field I/O Module identification.

3.10.9.1.1 Frame Types

The frame type shall be determined by the value of the first byte of the message. The command frames type values 112 – 127 (0x70 – 0x7F) and associated response frame type values 240 – 255 (0xF0 – 0xFF) are allocated for Manufacturer diagnostics. All other frame types not called out are reserved. The command-response Frame Type values and message times shall be as follows:

<table>
<thead>
<tr>
<th>Module Command</th>
<th>I/O Module Response</th>
<th>Description</th>
<th>Minimum Message Time</th>
<th>Maximum Message Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-43</td>
<td>128-171</td>
<td>Reserved for NEMA TS 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Module Command</td>
<td>I/O Module Response</td>
<td>Description</td>
<td>Minimum Message Time</td>
<td>Maximum Message Time</td>
</tr>
<tr>
<td>----------------</td>
<td>---------------------</td>
<td>--------------------------------------------------</td>
<td>----------------------</td>
<td>----------------------</td>
</tr>
<tr>
<td>44-48</td>
<td>172-176</td>
<td>Reserved</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>49</td>
<td>177</td>
<td>Request Module Status</td>
<td>250 µs</td>
<td>275 µs</td>
</tr>
<tr>
<td>50</td>
<td>178</td>
<td>MC Management</td>
<td>222.5 µs</td>
<td>237.5 µs</td>
</tr>
<tr>
<td>51</td>
<td>179</td>
<td>Configure Inputs</td>
<td>344.5 µs</td>
<td>6.8750 ms</td>
</tr>
<tr>
<td>52</td>
<td>180</td>
<td>Poll Raw Input Data</td>
<td>317.5 µs</td>
<td>320 µs</td>
</tr>
<tr>
<td>53</td>
<td>181</td>
<td>Poll Filtered Input Data</td>
<td>317.5 µs</td>
<td>320 µs</td>
</tr>
<tr>
<td>54</td>
<td>182</td>
<td>Poll Input Transition Buffer</td>
<td>300 µs</td>
<td>10.25 ms</td>
</tr>
<tr>
<td>55</td>
<td>183</td>
<td>Set Outputs</td>
<td>405 µs</td>
<td>410 µs</td>
</tr>
<tr>
<td>56</td>
<td>184</td>
<td>Configure Input Tracking</td>
<td>340 µs</td>
<td>10.25 ms</td>
</tr>
<tr>
<td>57</td>
<td>185</td>
<td>Configure Complex Outputs</td>
<td>340 µs</td>
<td>6.8750 ms</td>
</tr>
<tr>
<td>58</td>
<td>186</td>
<td>Reserved / Optional (Configure Watchdog)</td>
<td>222.5 µs</td>
<td>222.5 µs</td>
</tr>
<tr>
<td>59</td>
<td>187</td>
<td>Controller Identification</td>
<td>222.5 µs</td>
<td>222.5 µs</td>
</tr>
<tr>
<td>60</td>
<td>188</td>
<td>I/O Module Identification</td>
<td>222.5 µs</td>
<td>222.5 µs</td>
</tr>
<tr>
<td>61</td>
<td>189</td>
<td>Switch Pack Drivers</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>62</td>
<td>190</td>
<td>Send to Local Flash Command</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>63</td>
<td>191</td>
<td>Poll variable length raw input (see Section 3.10.9.1.2)</td>
<td>317.5 µs</td>
<td>320 µs</td>
</tr>
<tr>
<td>64</td>
<td>192</td>
<td>Variable length command outputs</td>
<td>405 µs</td>
<td>410 µs</td>
</tr>
<tr>
<td>65</td>
<td>193</td>
<td>Get CMU Configuration</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>66</td>
<td>---</td>
<td>Time and Date Command</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>67</td>
<td>195</td>
<td>Switch Pack Drivers</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>68-111</td>
<td>196-239</td>
<td>Reserved</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>112-127</td>
<td>240-255</td>
<td>Manufacturer Diagnostics</td>
<td>---</td>
<td>---</td>
</tr>
</tbody>
</table>

3.10.9.1.2 ITS Cabinet Monitor

Messages 61/189, 62/190, 65/193, 66 (no response) and 67/195 are for the ITS Cabinet Monitor Unit. See ITS Cabinet Standard, Section 4.4.16, Serial Bus #1 Frames (see Chapter 1.4 References in this standard).

Message 63/191 shall be identical to Message 52/180 except that Byte 2 of the Message 63 response shall denote the (variable) number of input data bytes contained in the response message.

Message 64/192 shall be identical to Message 55/183 except that Byte 2 of the Message 64 command shall denote the (variable) number of output data and control bytes contained in the command message.

3.10.9.2 Request Module Status

The Command shall be used to request FI/O Module status information response. Command/response frames are as follows:

**Request Module Status Command**

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 49)</td>
<td>0</td>
<td>0</td>
<td>0 1 1 0 0 0 1</td>
</tr>
<tr>
<td>Reset Status Bits</td>
<td>P</td>
<td>E</td>
<td>R</td>
</tr>
</tbody>
</table>

**Request Module Status Response**

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
</table>
### 3.10.9.2.1 Status Bits

The response Status Bits are defined as follows:

- **P** - Indicates FI/O hardware reset
- **E** - Indicates a communications loss of greater than 2 seconds
- **M** - Indicates an error with the MC interrupt
- **L** - Indicates an error in the LINESYNC
- **W** - Indicates that the FI/O has been reset by the Watchdog
- **R** - Indicates that the SCC Receive Error count byte has rolled over
- **T** - Indicates that the SCC Transmit Error count byte has rolled over
- **K** - Indicates the Datakey has failed or is not present

### 3.10.9.2.2 Request Module Status

Each of these bits shall be individually reset by a '1' in the corresponding bit of any subsequent Request Module Status frame, and the response frame shall report the current status bits. The SCC error count bytes shall not be reset. When an SCC error count rolls over (255 - 0), its corresponding roll-over flag shall be set.

### 3.10.9.3 MC Management

MC Management frame shall be used to set the value of the MC. The 'S' bit shall return status '0' on completion or '1' on error. The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

#### MC Management Command

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 50)</td>
<td>0 0 1 1 0 0 1 0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>New Timestamp MSB</td>
<td>x x x x x x x x</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>New Timestamp NMSB</td>
<td>x x x x x x x x</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>New Timestamp NLSB</td>
<td>x x x x x x x x</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>New Timestamp LSB</td>
<td>x x x x x x x x</td>
<td></td>
<td>5</td>
</tr>
</tbody>
</table>

#### MC Management Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 178)</td>
<td>1 0 1 1 0 0 1 0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Status</td>
<td>0 0 0 0 0 0 0 0</td>
<td>S</td>
<td>2</td>
</tr>
</tbody>
</table>

### 3.10.9.4 Configure Inputs Command

The Configure Inputs command frame shall be used to change input configurations. The command-response frames are as follows:
### Configure Inputs Command

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 51)</td>
<td>0</td>
<td>1</td>
<td>1 0 1</td>
</tr>
<tr>
<td>Number of Items (n)</td>
<td>n</td>
<td>n</td>
<td>n 1 n n 1 n</td>
</tr>
<tr>
<td>Item # - Byte 1</td>
<td>E</td>
<td>Input Number</td>
<td>Byte 3(I-1)+3</td>
</tr>
<tr>
<td>Item # - Byte 2</td>
<td>Leading edge filter (e)</td>
<td>Byte 3(I-1)+4</td>
<td></td>
</tr>
<tr>
<td>Item # - Byte 3</td>
<td>Trailing edge filter (r)</td>
<td>Byte 3(I-1)+5</td>
<td></td>
</tr>
</tbody>
</table>

### Configure Inputs Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 179)</td>
<td>1</td>
<td>0</td>
<td>1 0 1</td>
</tr>
<tr>
<td>Status</td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 0 S</td>
</tr>
</tbody>
</table>

Block field definitions shall be as follows:

- **E** - Ignore Input Flag. “1” = do not report transitions for this input, “0” = report transitions for this input
- **e** - A one-byte leading edge filter specifying the number of consecutive input samples which must be “0” before the input is considered to have entered to “0” state from “1” state (range 1 to 255, 0 = disabled)
- **r** - A one-byte trailing edge filter specifying the number of consecutive input samples which must be “1” before the input is considered to have entered to “1” state from “0” state (range 1 to 255, 0 = disabled)
- **S** - return status S = '0' on completion or '1' on error

### 3.10.9.5 Poll Raw Input Data

The Poll Raw Input Data frame shall be used to poll the FI/O for the current unfiltered status of all inputs. The response frame shall contain 8 bytes (2A) or 15 bytes of information indicating the current input status. The frames are as follows:

#### Poll Raw Input Data Command

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 52)</td>
<td>0</td>
<td>0</td>
<td>1 1 0 1 0 0</td>
</tr>
</tbody>
</table>

#### Poll Raw Input Data Response (2070-2A)

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 180)</td>
<td>1</td>
<td>0</td>
<td>1 1 0 1 0 0</td>
</tr>
<tr>
<td>Inputs I0 (lsb) to I7 (msb)</td>
<td>x</td>
<td>x</td>
<td>x x x x x x</td>
</tr>
<tr>
<td>Inputs I8 to I63</td>
<td>x</td>
<td>x</td>
<td>x x x x x x</td>
</tr>
<tr>
<td>Timestamp MSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x</td>
</tr>
<tr>
<td>Timestamp NMSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x</td>
</tr>
<tr>
<td>Timestamp NLSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x</td>
</tr>
<tr>
<td>Timestamp LSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x</td>
</tr>
</tbody>
</table>

#### Poll Raw Input Data Response (2070-8 via 2070-2B)

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 180)</td>
<td>1</td>
<td>0</td>
<td>1 1 0 1 0 0</td>
</tr>
<tr>
<td>Inputs I0 (lsb) to I7 (msb)</td>
<td>x</td>
<td>x</td>
<td>x x x x x x</td>
</tr>
</tbody>
</table>
3.10.9.6  Poll Filtered Input Data

The Poll Filtered Input Data frame shall be used to poll the FI/O for the current filtered status of all inputs. The response frame shall contain 8 bytes (2A) or 15 bytes of information indicating the current filtered status of the inputs. Raw input data shall be provided in the response for inputs that are not configured for filtering. The frames are as follows:

**Poll Filter Input Data Command**

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 53)</td>
<td>0</td>
<td>0</td>
<td>1 1 0 1 0 1</td>
</tr>
</tbody>
</table>

**Poll Filter Input Data Response (2070-2A)**

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 181)</td>
<td>1</td>
<td>0</td>
<td>1 1 0 1 0 1</td>
</tr>
<tr>
<td>Inputs I0 (lsb) to I7 (msb)</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x</td>
</tr>
<tr>
<td>Inputs I8 to I63</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x</td>
</tr>
<tr>
<td>Timestamp MSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x</td>
</tr>
<tr>
<td>Timestamp NMSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x</td>
</tr>
<tr>
<td>Timestamp NLSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x</td>
</tr>
<tr>
<td>Timestamp LSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x</td>
</tr>
</tbody>
</table>

**Poll Filter Input Data Response (2070-8 via 2070-2B)**

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 181)</td>
<td>1</td>
<td>0</td>
<td>1 1 0 1 0 1</td>
</tr>
<tr>
<td>Inputs I0 (lsb) to I7 (msb)</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x</td>
</tr>
<tr>
<td>Inputs I8 to I119</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x</td>
</tr>
<tr>
<td>Timestamp MSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x</td>
</tr>
<tr>
<td>Timestamp NMSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x</td>
</tr>
<tr>
<td>Timestamp NLSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x</td>
</tr>
<tr>
<td>Timestamp LSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x</td>
</tr>
</tbody>
</table>

3.10.9.7  Poll Input Transition Buffer

The Poll Input Transition Buffer frame shall poll the FI/O for the contents of the input transition buffer. The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:
Poll Input Transition Buffer Command

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 54)</td>
<td>0 0 1 1 0 1 1 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Block Number</td>
<td>x x x x x x x x</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Input Transition Buffer Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 182)</td>
<td>1 0 1 1 0 1 1 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Block Number</td>
<td>x x x x x x x x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of Entries (n)</td>
<td>x x x x x x x x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Item #</td>
<td>S</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Item # Timestamp NLSB</td>
<td>x x x x x x x x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Item # Timestamp LSB</td>
<td>x x x x x x x x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Status</td>
<td>0 0 0 0 0 C F E G</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timestamp MSB</td>
<td>x x x x x x x x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timestamp NMSB</td>
<td>x x x x x x x x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timestamp LSB</td>
<td>x x x x x x x x</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The entry types are depicted as follows:

**Input Transition Entry**

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transition Entry Identifier</td>
<td>S</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Timestamp NLSB</td>
<td>x x x x x x x x</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>Timestamp LSB</td>
<td>x x x x x x x x</td>
<td></td>
<td>3</td>
</tr>
</tbody>
</table>

**MC Rollover Entry**

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rollover Entry Identifier</td>
<td>1 1 1 1 1 1 1 1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Timestamp MSB</td>
<td>x x x x x x x x</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>Timestamp NMSB</td>
<td>x x x x x x x x</td>
<td></td>
<td>3</td>
</tr>
</tbody>
</table>

3.10.9.7.1 Active Input

Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. Bit definitions are as follows:

S     Indicates the state of the input after the transition
C     Indicates the 255 entry buffer limit has been exceeded
F     Indicates the transition buffer limit has been exceeded
G     Indicates the requested block number is out of monotonic increment sequence
E     Same block number requested, E is set in response

3.10.9.7.2 Block Number Byte
The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module. When the FI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer shall be re-sent to the CPU Module and the 'E' flag set in the status response frame. If it is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent. If the block number is not incremented by one, the status G bit shall be set. The block number received becomes the current number (even if out of sequence). The Block Number byte sent in the response block shall be the same as that received in the command block. Counter rollover shall be considered as a normal increment.

3.10.9.8 Set Outputs

The Set Outputs frame shall be used to command the FI/O to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to "1". If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set to "1". Loss of LINESYNC reference shall also be indicated in Module Status Response Frame. The output bytes depend upon field I/O module. These command and response frames are as follows:

Set Outputs Command (2070-2A)

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 55)</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Outputs O0 (lsb) to O7 (msb) Data</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x Byte 2</td>
</tr>
<tr>
<td>Outputs O8 to O63 Data</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x Bytes 3 to 9</td>
</tr>
<tr>
<td>Outputs O0 (lsb) to O7 (msb) Control</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x Byte 10</td>
</tr>
<tr>
<td>Outputs O8 to O63 Control</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x Bytes 11 to 17</td>
</tr>
</tbody>
</table>

Set Outputs Command (2070-8 via 2070-2B)

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 55)</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Outputs O0 (lsb) to O7 (msb) Data</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x Byte 2</td>
</tr>
<tr>
<td>Outputs O8 to O103 Data</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x Bytes 3 to 14</td>
</tr>
<tr>
<td>Outputs O0 (lsb) to O7 (msb) Control</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x Byte 15</td>
</tr>
<tr>
<td>Outputs O8 to O103 Control</td>
<td>x</td>
<td>x</td>
<td>x x x x x x x Bytes 16 to 27</td>
</tr>
</tbody>
</table>

Set Outputs Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 183)</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Status</td>
<td>0</td>
<td>0</td>
<td>0 L E</td>
</tr>
</tbody>
</table>

3.10.9.9 Configure Input Tracking Functions

The Configure Input Tracking Functions frame shall be used to configure outputs to respond to transitions on a specified input. Each Output Number identified by Item Number shall respond as configured to the corresponding Input Number identified by the same Item Number. Input to Output mapping shall be one to one. If a command results in more than 8 input tracking outputs being configured, the response V bit shall be set to ‘1’ and the command shall not be implemented. The command and response frames are as follows:

Configure Input Tracking Functions Command

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 56)</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Number of Items</td>
<td>Number of Items</td>
<td>0 0 Byte 2</td>
<td></td>
</tr>
</tbody>
</table>
Configure Input Tracking Functions Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 184)</td>
<td>1</td>
<td>0</td>
<td>1 1 1 0 0 0 0 0 Byte 1</td>
</tr>
<tr>
<td>Status</td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 0 0 V Byte 2</td>
</tr>
<tr>
<td>Timestamp MSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x Byte 3</td>
</tr>
<tr>
<td>Timestamp NMSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x Byte 4</td>
</tr>
<tr>
<td>Timestamp NL SB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x Byte 5</td>
</tr>
<tr>
<td>Timestamp LSB</td>
<td>x</td>
<td>x</td>
<td>x x x x x x Byte 6</td>
</tr>
</tbody>
</table>

### 3.10.9.9.1 Definitions

- **E** 
  - '1' - Enable input tracking functions for this output
  - '0' - Disable input tracking functions for this output

- **I** 
  - '1' - The output is OFF when input is ON, ON when input OFF
  - '0' - The output is ON when input is ON, OFF when input is OFF

- **V** 
  - '1' - The max. number of 8 configurable outputs has been exceeded
  - '0' - No error

Number of Items – The number of entries in the frame. If zero, all outputs currently configured for input tracking shall be disabled.

### 3.10.9.9.2 Timestamp Value

The timestamp value shall be sampled prior to the response frame.

### 3.10.9.9.3 Outputs Tracks Inputs

Outputs which track inputs shall be updated no less than once per ms. Input to output signal propagation delay shall not exceed 2 ms.

### 3.10.9.9.4 Number of Item

The “Number of Item” field is valid from 0 to 16 (most that is sent at one time is 8 enables and 8 disables). If processing a command resulting in more than 8 Input Tracking functions being enabled, none of the command shall be implemented and response message “V” bit set to 1. If an invalid output or input number is specified for a function, the FIOM software shall not do that function definition. It shall also not be counted toward the maximum of 8 input tracking function allowed. The rest of the message shall be processed. When an Input Tracking function is disabled, the output is set according to the most recently received Set Outputs Command. When an input tracking function for an output is superseded (redefined as either another input tracking function or as a complex output function) nothing shall be done with the output. The most recent value remains until the new function changes it.

### 3.10.9.10 Configure Complex Output Functions

The Configure Complex Output Functions frame shall be used to specify a complex output for one to eight of any of the outputs. If a Configure Complex Output Function command results in more than eight outputs being configured, the "V" bit in the response message shall be set to a ‘1’, and the command shall not be implemented. Two output forms shall be provided, single pulse and continuous oscillation. These output forms shall be configurable to begin immediately or on a specified input trigger and, in the case of continuous oscillation, to continue until otherwise configured or to oscillate only while gated active by a
specified input. If the command gate bit is active, the command trigger bit shall be ignored and the specified input shall be used as a gate signal. The command and response frames are as follows:

### Configure Complex Output Functions Command

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 57)</td>
<td>0 0 1 1 1 0 0 1</td>
<td></td>
<td>Byte 1</td>
</tr>
<tr>
<td>Number of Items</td>
<td></td>
<td>Number of Items</td>
<td>Byte 2</td>
</tr>
<tr>
<td>Item # - Byte 1</td>
<td>0</td>
<td>Output Number</td>
<td>Byte 7(I-1)+3</td>
</tr>
<tr>
<td>Item # - Byte 2</td>
<td></td>
<td>Primary Duration (MSB)</td>
<td>Byte 7(I-1)+4</td>
</tr>
<tr>
<td>Item # - Byte 3</td>
<td></td>
<td>Primary Duration (LSB)</td>
<td>Byte 7(I-1)+5</td>
</tr>
<tr>
<td>Item # - Byte 4</td>
<td></td>
<td>Secondary Duration (MSB)</td>
<td>Byte 7(I-1)+6</td>
</tr>
<tr>
<td>Item # - Byte 5</td>
<td></td>
<td>Secondary Duration (LSB)</td>
<td>Byte 7(I-1)+7</td>
</tr>
<tr>
<td>Item # - Byte 6</td>
<td>0</td>
<td>Input Number</td>
<td>Byte 7(I-1)+8</td>
</tr>
<tr>
<td>Item # - Byte 7</td>
<td>P W G E J F R L</td>
<td></td>
<td>Byte 7(I-1)+9</td>
</tr>
</tbody>
</table>

### Configure Complex Output Functions Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 185)</td>
<td>1 0 1 1 1 0 0 1</td>
<td></td>
<td>Byte 1</td>
</tr>
<tr>
<td>Status</td>
<td>0 0 0 0 0 0 0 V</td>
<td></td>
<td>Byte 2</td>
</tr>
<tr>
<td>Timestamp (MSB)</td>
<td>x x x x x x x</td>
<td></td>
<td>Byte 3</td>
</tr>
<tr>
<td>Timestamp (NMSB)</td>
<td>x x x x x x x</td>
<td></td>
<td>Byte 4</td>
</tr>
<tr>
<td>Timestamp (NLSB)</td>
<td>x x x x x x x</td>
<td></td>
<td>Byte 5</td>
</tr>
<tr>
<td>Timestamp (LSB)</td>
<td>x x x x x x x</td>
<td></td>
<td>Byte 6</td>
</tr>
</tbody>
</table>
3.10.9.10.1  Bit Field

The bit fields of the command frame are defined as follows:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>Enable complex output function for this output</td>
</tr>
<tr>
<td></td>
<td>'1' - enable complex output function for this output</td>
</tr>
<tr>
<td></td>
<td>'0' - disable complex output function for this output</td>
</tr>
<tr>
<td>J</td>
<td>During the primary duration, the output shall be written as a logic '1'. During the secondary duration, the output shall be written as a logic '0'.</td>
</tr>
<tr>
<td></td>
<td>'1' - During the primary duration, the output shall be written as a logic '1'. During the secondary duration, the output shall be written as a logic '0'.</td>
</tr>
<tr>
<td></td>
<td>'0' - During the primary duration, the output shall be written as a logic '0'. During the secondary duration, the output shall be written as a logic '1'.</td>
</tr>
<tr>
<td>Output Number</td>
<td>7-bit output number identifying outputs</td>
</tr>
<tr>
<td>Primary Duration</td>
<td>For single pulse operation, this shall determine the number of 'ticks' preceding the pulse. For continuous oscillation, this shall determine the length of the inactive (first) portion of the cycle.</td>
</tr>
<tr>
<td>Secondary Duration</td>
<td>For single pulse operation, this shall determine the number of 'ticks' the pulse is active. Subsequent to the secondary duration, the output shall return to the state set according to the most recently received Set Outputs command. For continuous oscillation, this shall determine the length of the active (second) portion of the cycle. 0 = hold output state until otherwise configured.</td>
</tr>
<tr>
<td>F</td>
<td>Trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.</td>
</tr>
<tr>
<td></td>
<td>'1' - The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.</td>
</tr>
<tr>
<td></td>
<td>'0' - The trigger or gate shall be derived from the raw input.</td>
</tr>
<tr>
<td>R</td>
<td>For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.</td>
</tr>
<tr>
<td></td>
<td>'1' - For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.</td>
</tr>
<tr>
<td></td>
<td>'0' - For triggered output, the output shall be triggered by an OFF-to-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON.</td>
</tr>
<tr>
<td>Input Number</td>
<td>7-bit input number identifying inputs 0 Up.</td>
</tr>
<tr>
<td>P</td>
<td>The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.</td>
</tr>
<tr>
<td></td>
<td>'1' - The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.</td>
</tr>
<tr>
<td></td>
<td>'0' - The output is configured for continuous oscillation.</td>
</tr>
<tr>
<td>W</td>
<td>It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.</td>
</tr>
<tr>
<td></td>
<td>'1' - It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.</td>
</tr>
<tr>
<td></td>
<td>'0' - Operation shall begin within 2 ms of the command receipt.</td>
</tr>
<tr>
<td>G</td>
<td>Operation shall be gated active by the specified input.</td>
</tr>
<tr>
<td></td>
<td>'1' - Operation shall be gated active by the specified input.</td>
</tr>
<tr>
<td></td>
<td>'0' - Gating is inactive.</td>
</tr>
<tr>
<td>L</td>
<td>The LINESYNC based clock shall be used for the time ticks.</td>
</tr>
<tr>
<td></td>
<td>'1' - The LINESYNC based clock shall be used for the time ticks.</td>
</tr>
<tr>
<td></td>
<td>'0' - The MC shall be used for the time ticks.</td>
</tr>
<tr>
<td>V</td>
<td>Indicates maximum number of configurable outputs is exceeded.</td>
</tr>
<tr>
<td></td>
<td>'1' - Indicates maximum number of configurable outputs is exceeded.</td>
</tr>
<tr>
<td></td>
<td>'0' - No error</td>
</tr>
<tr>
<td>Number of items</td>
<td>The number of entries in the frame. If 0, all outputs currently configured as complex outputs shall be disabled.</td>
</tr>
</tbody>
</table>

3.10.9.10.2  Controlling Input Signals

Controlling input signals shall be sampled at least once per millisecond.
3.10.9.10.3 Number of Items

The “Number of Items” field is valid from 0 to 16. Zero means disable all Complex Output functions. Sixteen is the maximum because the most that is sent at one time is 8 enables and 8 disables. If processing a command results in more than 8 Complex Output functions being enabled, none of the command shall be implemented and the response message “V” bit shall be set to 1. If an invalid output or input number (the “G” or “W” bits being set to 1 is specified for a function, that function definition is not done by the FIOM software. It shall also not be counted towards the maximum of 8 Complex Output functions allowed. The rest of the message shall be processed. When a Complex Output function is disabled, the output is set according to the most recently received Set Outputs command. When a complex output function for an output is superseded, that is, redefined as wither another Complex Output function, or as an Input Tracking function, nothing special is done with the output. The most recent value remains until the new function changes it. The “G” bit (gating) set to 1 takes precedence over the “W” bit (triggering). If gating is ON, triggering is turned OFF, regardless of the value of the “W” bit in the command message. If a Complex Output is configured with the “G” bit set to 1 (gating) and the “P” bit set to 0 (continuous oscillation), the output is set to OFF (0) whenever the specified input changes state so that the oscillation should cease (output inactive). For a single pulse operation (“G” bit set to 1), after the secondary duration completes the Complex Output function shall be disabled, and the output shall be set according to the most recently received Set Outputs command.

3.10.9.11 Configure Watchdog

The Configure Watchdog frames shall be used to change the software watchdog timeout value. The Command and response frames are as follows:

<table>
<thead>
<tr>
<th>Description</th>
<th>Type Number = 58</th>
<th>msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timeout Value</td>
<td></td>
<td>0</td>
<td>0</td>
<td>1 1 0 1 0 1 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
<th>Type Number = 186</th>
<th>msb</th>
<th>Isb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Status</td>
<td></td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 0 Y</td>
</tr>
</tbody>
</table>

3.10.9.11.1 Timeout Value

The timeout value shall be in the range between 10 to 100 ms. If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.

3.10.9.11.2 Watchdog Timeout Value

On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the “Y” bit set. The response frame bit (Y) shall indicate a ‘1’ if the watchdog has been previously set and a ‘0’ if not.

3.10.9.12 Controller Identification
This is a legacy message command / response for FI/O modules with Datakey resident. Upon command, a response frame containing the 128 bytes of the Datakey. On NRESET transition to High or immediately prior to any interrogation of the Datakey, the FI/O shall test the presence of the Key. If absent, the FI/O Status Bit "K" shall be set and no interrogation shall take place. If an error occurs during the interrogation, Bit “K” shall be set. If “K” bit set, only the first two bytes shall be returned. The Command Response frames are as follows:

### Controller Identification Command

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 59)</td>
<td>0</td>
<td>0</td>
<td>1 1 1 0 1 1</td>
</tr>
</tbody>
</table>

### Controller Identification Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 187)</td>
<td>1</td>
<td>0</td>
<td>1 1 1 0 1 1</td>
</tr>
<tr>
<td>Status</td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 0 0</td>
</tr>
<tr>
<td>Datakey</td>
<td>x</td>
<td>x</td>
<td>x x x x x x</td>
</tr>
</tbody>
</table>

#### 3.10.9.13 Module Identification

The Field I/O Identification command frame shall be used to request the FI/O Identification. A value Response of “1” for the 2070-2A, “2” for the 2070-8, and “3” for 2070-2N. Response values 32 to 40 are reserved for the ITS Cabinet. The command and response frames are shown as follows:

### I/O Module Identification Command

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 60)</td>
<td>0</td>
<td>0</td>
<td>1 1 1 0 0</td>
</tr>
</tbody>
</table>

### I/O Module Identification Response

<table>
<thead>
<tr>
<th>Description</th>
<th>msb</th>
<th>lsb</th>
<th>Byte Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Type Number = 188)</td>
<td>1</td>
<td>0</td>
<td>1 1 1 0 0</td>
</tr>
<tr>
<td>FI/O ID byte</td>
<td>x</td>
<td>x</td>
<td>x x x x x x</td>
</tr>
</tbody>
</table>
3.11 Model 2070-3 Front Panel Assembly (FPA)

3.11.1 Model 2070-3 Front Panel Assembly

The Model 2070-3 Front Panel Assembly shall be delivered with one of the three options as called out under Section 3.8 General Controller Unit or in a contract's special provisions (governs). All options shall consist of a panel with latch assembly and two TSD #1 hinge attaching devices, assembly PCB, external serial port connectors (DB9 and RJ-45), CPU_ACTIVE LED indicator, and FP Harness Interface. The options shall include the additional features, as follows:

- **OPTION 3A** - FPA controller, two keyboards, AUX switch, alarm bell & Display A.
- **OPTION 3B** - FPA controller, two keyboards, AUX switch, alarm bell & Display B.
- **OPTION 3C** - System Serial Port 6 Lines, isolated and vectored to Connector C60P.
- **OPTION 3D** - FPA controller, two keyboards, AUX switch, alarm bell & Display D

3.11.2 Keyboards

Two Keyboards shall be provided, one with sixteen keys for hexadecimal (Hex) alphanumeric entry and the other with twelve keys to be used for cursor control and action symbol entry. Each key shall be engraved or embossed with its function character. Each key shall have an actuation force between 1.764 ounce and 3.527 ounce and provide a positive tactile indication of contact closure. Key contacts shall be hermetically sealed, have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact closure.

3.11.3 CPU_ACTIVE LED Indicator

The cathode of the CPU_ACTIVE LED Indicator shall be electrically connected to the CPU_ACTIVE signal and shall be pulled up to +5 VDC.

3.11.4 Display Liquid Crystal Display (LCD)

The Display shall consist of a Liquid Crystal Display (LCD), a backlight, and a contrast potentiometer control. Display A shall have 4 lines of 40 characters each with minimum character dimensions of 0.197 in. wide by 0.411 in. high and an electro-luminescent (EL) backlight. Display B shall have 8 lines of 40 characters each with minimum dimensions of 0.104 in. wide by 0.167 in. high and either LED or EL backlight. Display D shall have 16 lines of 40 characters each with minimum dimensions of 0.104 in wide by 0.167 in high and either LED or EL backlight.

3.11.4.1 Characters and Angles of Liquid Crystal Display (LCD)

Each character shall be composed of a 5x7 dot matrix with a underline row or a 5x8 dot matrix. The viewing angle of the LCD shall be optimized for direct (90°) viewing, ±35° vertical, ±45° horizontal. The LCD shall have variable contrast with a minimum ratio of 4:1. The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

3.11.4.2 Backlight

The backlight shall be turned on and off by the Controller Circuitry. The backlight and associated circuitry shall consume no power when in off state. A potentiometer shall control the LCD contrast with clockwise rotation increasing contrast. The contrast shall depend on the angular position of the potentiometer, which shall provide the entire contrast range of the LCD.

3.11.4.3 Cursor Display
Cursor display shall be turned ON and OFF by command. When ON, the cursor shall be displayed at the current cursor position. When OFF, no cursor shall be displayed. All other cursor functions (positioning, etc.) shall remain in effect.

3.11.5 FPA Controller

The FPA Controller shall function as the Front Panel Device controller interfacing with the CPU Module.

3.11.5.1 FPA Reset

A FPA Reset Switch shall be provided on the Assembly PCB. The momentary Control switch shall be logic OR'd with the CPU_Reset Line, producing a FPA Reset Output. Upon FPA Reset being active or receipt of a valid Soft Reset display command, the following shall occur:

- Auto-repeat, blinking, auto-wrap, and auto-scroll shall be set to OFF.
- Each special character shall be set to ASCII SPC (space).
- The tab stops shall be set to columns 9, 17, 25, and 33.
- The backlight timeout value shall be set to 6 (60 seconds).
- The backlight shall be extinguished.
- The display shall be cleared (all ASCII SPC).
- The cursor display shall be turn OFF.
- The FPA module shall transmit a power up string through /sp6 to the CPU once power is applied to the FPA, or the FPA hardware Reset Button is pushed. The string is " ESC [ PU", Hex value “1B 5B 50 55”.

3.11.5.2 Key Press

When a key press is detected, the appropriate key code shall be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code shall be sent. If a key is depressed while another key is depressed, no additional code shall be sent.

3.11.5.3 Auto Repeat

Auto-repeat shall be turned ON and OFF by command. When ON, the key code shall be repeated at a rate of 5 times per second starting when the key has been depressed continuously for 0.5 second, and shall terminate when the key is released or another key is pressed.

3.11.5.4 AUX

When the AUX Switch is toggled, the appropriate AUX Switch code shall be transmitted to the CPU.

3.11.5.5 Controller Circuitry

The controller circuitry shall be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination with the standard ASCII characters. Undefined characters shall be ignored. User-composed characters shall be represented in the communication command codes on Page A9-12. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the top pixel in a column and the least significant bit shall represent the bottom pixel. A logic ‘1’ shall turn the pixel ON. There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an ”f.” If the number of Pn's is more than the number of columns available on the LCD, the extra Pn's shall be ignored. P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.
3.11.5.6 Character Overwrite

Character Overwrite mode shall be the only display mode supported. A displayable character received shall always overwrite the current cursor position on the Display. The cursor shall automatically move right one character position on the Display after each character write operation. When the rightmost character on a line (position 40) has been overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.

3.11.5.7 Auto Wrap

Auto-Wrap shall be turned ON & OFF by command. When ON, a new line operation shall be performed after writing to position 40. When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.

3.11.5.8 Cursor Positioning

Cursor positioning shall be non-destructive. Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.

3.11.5.9 Blinking Characters

Blinking characters shall be supported, and shall be turned ON and OFF by command. When ON, all subsequently received displayable characters shall blink at the rate of 1 Hz with a 60% ON / 40% OFF duty cycle. It shall be possible to display both blinking and non-blinking characters simultaneously.

3.11.5.10 Tab Stops

Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.

Tab stops shall be set based only upon the column (horizontal) position of the cursor; the row position shall be ignored. Each tab that is set shall apply to all rows of the display. In this way, tabs shall operate similarly to a typewriter or line printer. For example, if the cursor is positioned at column 21, row 3 when a Set Tab Stop command (ESC H) is received, a tab stop is placed at column 21 and applies to every row of the display. If the cursor is then positioned to column 21, row 5, and a Clear Tab Stop command (ESC[0g) is received, the tab stop on column 21 is removed and there will be no tab stop on any row of the display at that column position.

3.11.5.11 Auto Scroll

Auto-scroll shall be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one line. When OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.

3.11.5.12 Displayable Characters

Displayable characters shall be refreshed at least 20 times per second.
3.11.5.13 Display Back Light Illuminate

The Display back light shall illuminate when any key is pressed and shall illuminate or extinguish by command. The backlight shall extinguish when no key is pressed for a specified time. This time shall be program selected by command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals. A value of 1 shall correspond to a timeout interval of 10 seconds. A value of 0 shall indicate no timeout.

3.11.5.14 Command Codes

The Command Codes shall use the following conventions:

1. Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows:
   - Pn: Value parameter, to be replaced by a value, using one ASCII character per digit without leading zeros.
   - P1: Ordered and numbered parameter. One of a listed known parameters with a specified order and number (Continues with P2, P3, etc.)
   - Px: Display column number (1-40), using one ASCII character per digit without leading zero.
   - Py: Display line (1-4) one ASCII character
   - ... : Continue the list in the same fashion
   
   Values of 'h' (0x68) and 'l' (0x6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).

2. ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.

3. Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 0x00 to 0x7F (7 bits).

3.11.5.15 Controller Circuit

The Controller Circuit shall communicate via a SP6 asynchronous serial interface. The interface shall be configured for 38.4 kbps, 8 data bits, 1 stop bit, and no parity.

3.11.5.16 C50 Enable Function

C50 ENABLE function when grounded by Connector C50 Pins 1 and 5 shall be brought to Connector A1 Pin B21 for the purpose of disabling the module Channel 2.

3.11.6 Front Panel

The Front Panel shall include an electronic bell to signal receipt of BEL character (0x07). The bell shall sound at 2,000 Hz, with a minimum output rating of 85 dB at a distance of 4 feet, for 350 ±100 ms upon receipt of BEL character (0x07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.
3.12 Model 2070-4 Power Supply Module

3.12.1 Model 2070-4 Power Supply Module

The Model 2070-4 Power Supply Module shall be independent, self-contained Module, vented, and cooled by convection only. The Module shall slide into the unit’s power supply compartment from the back of the Chassis and be attached to the Backplane Mounting Surface by its four TSD #3 Devices.

3.12.2 On/Off Power Switch

An "On/Off" POWER Switch, four LED DC Power Indicators, Power Supply Receptacle POWER Connectors, and the Incoming AC Fuse protection shall be provided on the Module Front. The LED DC POWER Indicators shall indicate all required DC voltages meet the following conditions: the +5 VDC and 12 VDC are within 5% and of their nominal levels.

3.12.3 Input Protection

Two 0.5 Ω, 10 W wire-wound power resistors with a 0.2 µH inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arresters shall be provided between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 µF capacitor shall be placed between AC+ & AC- (between the resistor & arresters).

3.12.4 +5 VDC Standby Power

+5 VDC Standby Power shall be provided to hold up specified circuitry during the power down period. It shall consist of the monitor circuitry; hold up capacitors, and charging circuitry. A charging circuit shall be provided, that under normal operation, shall fully charge and float the capacitors consistent with the manufacturers’ recommendations. The Hold Up power requirements shall be a minimum constant drain of 600 µA at a range of +5 to +2 VDC for over 600 minutes.

3.12.5 Monitor Circuitry

Monitor Circuitry shall be provided to monitor incoming AC Power for Power Failure and Restoration and LINESYNC generation.

3.12.5.1 AC Fail/Power Down Output Lines

The AC Fail/Power Down Output Lines shall go Low (ground true) immediately upon Power Failure. The Lines shall transition to High within 50 ms after both Power Restoration and supply is fully recovered. The Lines shall be driven separately. The Sysreset/Powerup Output Lines shall transition to Low 525 +/- 25 ms after AC Fail/Power Down transition to Low. The Lines shall transition to HIGH 225 +/- 25 ms after both Power Restoration and the supply is fully recovered. The Lines shall be driven separately.

3.12.5.2 Monitor Circuitry

The monitor circuitry shall switch the +5 VDC Standby ON immediately upon Power Failure and isolate (OFF) the line at Power Up.

3.12.5.3 60 Hz Square Wave LINESYNC

The 60 Hz Square Wave LINESYNC signal shall be generated by a crystal oscillator, which shall synchronize to the 60-Hz VAC incoming power line at 120 and 300 degrees. A continuous square wave signal shall be +5 VDC amplitude, 8.333 ms half-cycle pulse duration, and 50 ± 1% duty cycle. The output shall have drive sink capability of 16 mA. A 2 K-Ohm pull-up resistor shall be connected between the output and +5 VDC. The monitor circuit shall compensate for missing pulses and line noise during
normal operation.

3.12.5.4 Linesync

The Linesync shall continue until Sysreset transitions Low and begin then Sysreset transitions High.

3.12.6 Power Supply Requirements

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Minimum Load</th>
<th>Maximum Load</th>
<th>Load Reg.</th>
<th>Line Reg.</th>
<th>Ripple &amp; Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5 VDC</td>
<td>0.0 A</td>
<td>10.0 A</td>
<td>± 5%</td>
<td>± 1%</td>
<td>50 mV P-P</td>
</tr>
<tr>
<td>+12 VDC Serial</td>
<td>0.0 A</td>
<td>0.5 A</td>
<td>± 5%</td>
<td>± 1%</td>
<td>50 mV P-P</td>
</tr>
<tr>
<td>-12 VDC Serial</td>
<td>0.0 A</td>
<td>0.5 A</td>
<td>± 5%</td>
<td>± 1%</td>
<td>50 mV P-P</td>
</tr>
<tr>
<td>+12 VDC</td>
<td>0.0 A</td>
<td>1.0 A</td>
<td>± 5%</td>
<td>± 1%</td>
<td>50 mV P-P</td>
</tr>
</tbody>
</table>

3.12.6.1 Line / Load Regulation

The Power Supply Module shall meet Line/Load Regulation for input voltage range of 90 to 135 VAC, minimum and maximum loads called out in the table including ripple and noise.

3.12.6.2 Efficiency

70% minimum.

3.12.6.3 Ripple & noise

Less than 0.2% RMS, 1% peak to peak, or 50 mV, whichever is greater.

3.12.6.4 Voltage Overshoot

No greater than 5 %, all outputs.

3.12.6.5 Over Voltage Protection

130% Vout for all outputs.

3.12.6.6 Circuit Protection

Automatic recovery upon removal of fault.

3.12.6.7 Inrush Current

Cold Start Inrush shall be less than 25 A at 115VAC.

3.12.6.8 Transient response

Output voltage back to within 1% in less than 500 µs on a 50% Load change. Peak transient not to exceed 5%. 
3.12.6.9  Holdup Time

The power supply shall supply 30 W minimum for 550 ms after ACFAIL going LOW. The supply shall be capable of holding up the Unit for two 500 ms Power Loss periods occurring in a 1.5-second period.

3.12.6.10  Remote Sense

+5 VDC compensates 250 mV total line drop. Open sense load protection required.
3.13 Unit Chassis and Model 2070-5 VME Cage Assembly

3.13.1 General

The Chassis shall consist of the metal housing, Serial Motherboard, Back-plane Mounting Surface, Power Supply Module Supports, slot card guides, Wiring Harnesses, and Cover Plate(s). All external screws shall be countersunk and shall be Phillips flat head stainless steel type. The housing shall be treated with clear chromate and the slot designation labeled on the back-plane mounting surface above the upper slot card guide. The Chassis shall be cooled by convection only. The top and bottom pieces of the housing shall be slotted for vertical ventilation.

3.13.2 Serial Motherboard

Serial Motherboard shall function as support for its connectors, A1 to A5 and FP, and as the interface between the CPU and the dedicated modules/Front Panel carrying both serial communications, logic, and power circuits. The PCB shall be multi-layered, with one layer plane assigned to DC Ground. A wiring harness PS2 shall be provided between the Model 2070-4 Power Supply and the Motherboard PCB (provide strain relief). Test points shall be provided on the FPA side of the Motherboard for PS2 lines. A wiring harness FP shall be provided, linking the Motherboard with the FPA.

3.13.3 Model 2070-5 VME Cage Assembly

MODEL 2070-5 VME Cage Assembly shall consist of 3U five slot/connector VME Cage, Front Mounting Plate, and PS1 Harness. The VME Cage shall conform to VME Standard IEEE P1014/D12 and ANSI/VITA 1-1994 for 3U Cage. All slot/connectors shall be A24: D16 Interface.
3.14 Model 2070-6 A & B Async/Modem Serial Communication Modules

3.14.1 Fuse Isolation

A fused isolated +5 VDC with a of 100 mA power supply shall be provided for external use.

Option – BOURNS MF – MSMD020 PTC (Positive Temperature Coefficient) Resettable Fuse allowed.

3.14.2 Half & Full Duplex Switch

A switch shall be used to vertically switch between Half-Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.

3.14.3 Circuits

Two independent circuits designated Circuits #1 and Circuits #2, shall be provided. Both circuit functions shall be identical, except for their Serial Communications Port and external connector (Circuits #1 to SP1 [or SP3] and C2S Connector and Circuits #2 to SP2 [or SP4] and C20S Connector). Circuits #1 & #2 shall optically isolate the FSK, C2 and C20 Serial Ports from the Motherboard SP EIA-495 signals. Each circuit shall provide full isolation from each other and the Model 2070 Motherboard. Line drivers/receivers shall be socket or surface mounted.

The 2070-6x module’s isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, whichever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

3.14.4 Modem

Each circuit shall have a common power independent Modem with the following requirements:

- **Modulation**: Phase coherent frequency shift keying (FSK).
- **Data Format**: Asynchronous, serial by bit.
- **Line & Signal Requirements**: Type 3002 voice-grade, unconditioned Tone Carrier Frequencies (Transmit and Receive), MARK and SPACE: ±1% tolerance. The operating band shall be (half power, -3 dB) between 1.0 KHz & 2.4 KHz for 2070-6A and 9.9 KHz & 18.9 KHz for 2070-6B.
- **Transmitting Output Signal Level**: 0, -2, -4, -6, and -8 dB (at 1.7 KHz for 2070-6A and 14.7 KHz for 2070-6B) continuous or switch selectable.
- **Receiver Input Sensitivity**: 0 to -40 dB.
- **Receiver Bandpass Filter**: Shall meet the error rate requirement specified below and shall provide 20dB/octave, minimum active attenuation for all frequencies outside the operating band.
- **Clear-to-Send (CTS) Delay**: 11 ±3 ms.
- **Receive Line Signal Detect Time**: 8 ±2 ms mark frequency.
- **Receive Line Squelch**: 6.5 (±1) ms, 0 ms (OUT).
- **Soft Carrier Turn Off Time**: 10 ±2 ms. When the RTS is unasserted; the carrier shall turn off or go to soft carrier frequency.
Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.

Error Rate: Shall not exceed 1 bit in 100 kb, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3,000 Hz band.

Transmit Noise: Less than -50 dB across 600 Ω resistive load within the frequency spectrum of 300 to 3,000 Hz at maximum output.

Modem interface: EIA-232 Standards.

Frequencies and Data Rates:

<table>
<thead>
<tr>
<th>Model</th>
<th>Mark Hz</th>
<th>Space Hz</th>
<th>Soft Carrier Hz</th>
<th>Data Rate bps</th>
</tr>
</thead>
<tbody>
<tr>
<td>2070-6A</td>
<td>1200</td>
<td>2200</td>
<td>900</td>
<td>300 - 1200</td>
</tr>
<tr>
<td>2070-6B</td>
<td>11200</td>
<td>17600</td>
<td>7800</td>
<td>300 - 9600</td>
</tr>
</tbody>
</table>

3.14.5 Enable/Disable Feature

The 2070-6x modules shall provide circuitry to disable their Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable Channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on these modules.

3.14.6 Hot Swappable

The 2070-6x module shall be “Hot” swappable without damage to its circuitry or operations. A communication “glitch” occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.
3.15 Model 2070-7A Async Serial Comm Module

3.15.1 Circuits

Two opto-isolated independent circuits designated circuits #1 (Channel 1) and circuits #2 (Channel 2), shall be provided. Their functions are identical, except for the CPU Serial Communications Port and external connector (circuits #1 to SP1 [or SP3] and Connector C21S and circuits #2 to SP2 [or SP4] and Connector C22S). Line drivers/receivers shall be socket or surface mounted.

The 2070-7x module’s isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, whichever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

3.15.2 2070-7A

Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground; and drive / receive external EIA-232 devices via C21 / C22 Connectors. Each connector shall be DB-9S type.

3.15.3 LED Indicator

Each circuit signal TX and RX line shall have an LED Indicator mounted on the front plate and labeled according to function.

3.15.4 Enable/Disable Features

Each 2070-7x module shall provide circuitry to disable its Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable Channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on the module.

Each 2070-7x module shall provide circuitry to manually disable its Channel 1. When Channel 1 is manually disabled, the “Ch. A Disable” LED indicator shall be turned ON.

3.15.5 Hot Swappable

Each 2070-7x module shall be “Hot” swappable without damage to its circuitry or operations. A communication “glitch” occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.
3.16 Model 2070-9D Dial-Up Modem Comm Module

3.16.1 2070-9D Modem

The Model 2070-9D Modem shall consist of a Dial-Up Modem and shall be a Plug-in Card style version for the 2070 Controller.

3.16.2 Dial-Up Modem

The Dial-Up Modem shall consist of a 33.6 kbps dial-up modem meeting the V.34 AT Command set standard. The Modem shall contain two RJ-11 connectors, one designated as the Line and the second as Phone. An internal speaker shall be provided as an indicator for phone call progress. The speaker shall be controlled through AT standard commands. Front Panel LED indicators shall also be provided as shown in the Figure A-19 Model 2070-9D Dial-Up Modem Comm Module of these specifications.

3.16.2.1 Modem Default Configuration

The Modem shall contain the following default configurations:

**ACTIVE PROFILE:**
B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0 &T5 &X0 &Y0

<table>
<thead>
<tr>
<th>S00:001</th>
<th>S11:095</th>
</tr>
</thead>
<tbody>
<tr>
<td>S01:000</td>
<td>S12:050</td>
</tr>
<tr>
<td>S02:043</td>
<td>S18:000</td>
</tr>
<tr>
<td>S03:013</td>
<td>S25:005</td>
</tr>
<tr>
<td>S04:010</td>
<td>S26:001</td>
</tr>
<tr>
<td>S05:008</td>
<td>S36:007</td>
</tr>
<tr>
<td>S06:002</td>
<td>S38:020</td>
</tr>
<tr>
<td>S07:050</td>
<td>S46:138</td>
</tr>
<tr>
<td>S08:002</td>
<td>S48:007</td>
</tr>
<tr>
<td>S09:006</td>
<td>S95:000</td>
</tr>
<tr>
<td>S10:014</td>
<td></td>
</tr>
</tbody>
</table>

**STORED PROFILE 0:**
B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0 &T5 &X0

<table>
<thead>
<tr>
<th>S00:001</th>
<th>S12:050</th>
</tr>
</thead>
<tbody>
<tr>
<td>S02:043</td>
<td>S18:000</td>
</tr>
<tr>
<td>S06:002</td>
<td>S36:007</td>
</tr>
<tr>
<td>S07:050</td>
<td>S40:104</td>
</tr>
<tr>
<td>S08:002</td>
<td>S41:195</td>
</tr>
<tr>
<td>S09:006</td>
<td>S46:138</td>
</tr>
<tr>
<td>S10:014</td>
<td>S95:000</td>
</tr>
<tr>
<td>S11:095</td>
<td></td>
</tr>
</tbody>
</table>

Profile 0 should be configured as shown above and default as the active profile on wake up. Factory default shall wake up at 2400 Baud, Parity 8, N, 1 and no handshaking.

The Modem shall have a switch (S1) and shall be factory configured as follows:

<table>
<thead>
<tr>
<th>S1 DESCRIPTION</th>
<th>OPEN</th>
<th>CLOSE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Modem Select</td>
<td>Smart Modem</td>
<td>Lock</td>
</tr>
</tbody>
</table>
Each switch shall be OPEN as factory default except for position #2, which shall be closed as default. User shall be able to disable the SMART Modem Mode and set user baud rate, handshaking, and parity.

### 3.16.2.2 Modulation

The Dial-Up Modem shall use Quadrature Amplitude Modulation and operate within the following frequencies:

- Data Carrier 1800 ± 0.5 Hz
- Calling Tone 1300 ± 10 Hz
- Answering Tone 2100 ± 15 Hz

The Modem shall have Receiver Frequency Tolerance of ± 14 Hz

### 3.16.2.3 Modem Standards

The Dial-Up Modem shall be ITU V.90, V.34 and Rockwell V.FC compatible. It shall meet the standards:

- V.90, V.34, V.32 bis, V.22 bis, V.22A/B, V.23, V.21, Bell 212, Bell 103, V.33, V.17, V.29, V.27 ter, and V.21 Channel 2.

### 3.16.2.4 Data Rates

The Dial-Up Modem shall support the following data rates:

- 33.6 kbps, 31.3 kbps, 28.8 kbps, 26.4 kbps, 24.0 kbps, 21.6 kbps, 19.2 kbps, 16.8 kbps, 14.4 kbps, 12.0 kbps, 9.6 kbps, 7.2 kbps, 4.8 kbps, 2.4 kbps, 1.2 kbps, and 300 baud.

The Modem shall automatically select the best operating speed as indicated in Section 3.16.2.1 Modem Default Configuration of these specifications.

### 3.16.2.5 Error Correction & Data Compression

The Modem shall use V.42 LAPM, MNP2-4 and MNP 10 for error correction and V.42 Bis, MNP 5 for Data Compression.

### 3.16.2.6 Tx/Rx Power Level

The transmit level shall be fixed at -11 ± 2 dB and the receiver shall have a S/N Ratio of -26 dB with a Dynamic Range of 12 dBm to -42 dBm.

The Ring detect Sensitivity shall be 38 V RMS.

### 3.16.2.7 Line Interface

The Dial-Up Modem shall have a Ring Equivalent of 1 Bel and a terminating Impedance of 600 Ω. It shall have return loss of better than 14 dB.

### 3.16.3 Circuit
The Model 2070-9D shall be provided with full isolation from the Model 2070 Motherboard. Line drivers/receivers shall be socket or surface mounted.

The 2070-9D module’s isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1 Mbps, whichever is less.

3.16.4 Hot Swappable

The 2070-9D Module shall be “Hot” swappable without damage to its circuitry or operations. A communication “glitch” occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.

3.16.5 Power Requirements

The power requirements of the Model 2070-9D Modem shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

3.16.6 Environmental

The Model 2070-9D Modem shall operate within the specifications listed in Section 3.7.4.

3.16.7 Form Factor

See Figure A-19 Model 2070-9D Dial-Up Modem Comm Module for Details
3.17 NEMA 2070

3.17.1 2070 / NEMA Standard Controller Units

This specification covers two versions of 2070 / NEMA Standard Controller Units. The versions associate with NEMA TS 1/TS 2 Type 2 and NEMA TS 2 Type 1 Standards. They are as follows:

Model 2070E N1 Controller Unit (TS 1/TS 2 Type 2)
Model 2070E N2 Controller Unit (TS 2 Type 1)

3.17.2 N1 Unit Consisting

The Model 2070E N1 Controller Unit consists of:

- **Unit Chassis**
  - 2070-1E CPU Module
  - 2070-2B Field I/O Module
  - 2070-3B Front Panel Module
  - 2070-4N (A) Power Supply Module
  - 2070-5 VME Cage Assembly (if required)
  - 2070-8 Field I/O Module

3.17.3 N2 Unit Consisting

The MODEL 2070E N2 CONTROLLER UNIT consists of:

- **Unit Chassis**
  - 2070-1E CPU Module
  - 2070-2N Field I/O Module
  - 2070-3B Front Panel Module
  - 2070-4N (A) Power Supply Module
  - 2070-5 VME Cage Assembly (if required)

3.17.4 Address

The Serial Port 5 Frame Address for 2070-2N and 2070-8 shall be “20”.

3.17.5 Sheet Metal Tolerance

Sheet metal tolerance shall be 0.015 in or less for Modules 2070-2N, 2070-4N, and 2070-8.
3.18  2N Field I/O Module

3.18.1  2070-2N Field I/O Module

The 2070-2N Field I/O Module provides a TS 2 Type 1 compatible SDLC interface via 2070 Serial Port 3, AC Power to the 2070 Unit and Fault Monitor LOGIC Output via SP5 on output O78 (similar to the 2070-8) to the NEMA TS 2 Malfunction Management Unit (MMU). The communications timeout operation shall function in a manner similar to the 2070-8 (see Sections 3.20.11.6 and 3.10.11.7 for details).

3.18.2  Requirements Exceptions

The Module shall meet the 2070–2A Module Requirements with the following exceptions:

- No C1, C11 and C12 Connectors on the front panel of the module
- No 64 inputs / 64 outputs requirements
- Serial Port 5 routed to the FCU MPU Device only
- Serial Port 3 shall not have a disabling switch
- No Watchdog output
- No Muzzle Shunt

3.18.3  Types

The module shall be a 4X type board/front panel with three connectors. The connectors are 10 Pin Connector A, a NEMA 5-15 Receptacle and a Port 1 DA-15S connector labeled as either “C15S” or “Port 1”. The Port 1 (C15S) connector shall be a 15 pin metal shell DA-15 connector with female contacts. The connector shall be equipped with latching blocks and shall intermate with a 15 pin D type connector, Amp Incorporated part number 205206-1, or equivalent, which is equipped with spring latches, Amp Incorporated part number 745012-1, or equivalent.

3.18.4  Power

Incoming 2070 AC Power is derived from Connector A Pin C (AC+), Pin A (AC-), and Pin H (Equipment Ground). The power is directly routed to the NEMA 5-15 Receptacle with equipment ground also connected to the face plate. Connector A shall intermate with a NEMA TS 2 Type 1 (MS3106( )-18-1S) cable.

3.18.5  Isolation

The module shall isolate 2070 Serial Port 3 from the A3 Connector and reconvert the lines to external EIA 485 drivers/receivers which shall be terminated at C15S Connector. The Port shall be clocked at 153.6 kbps.

3.18.6  FCU Output

An FCU output shall drive an open collector transistor whose output shall be routed to Connector A Pin F for use as a FAULT MONITOR Output. The transistor shall be capable of sinking 200 mA at 30 VDC.

3.18.7  Connectors A, C15S pin out and functions

Connectors A and C15S pin out and functions are as follows:
## CONNECTOR A

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
<th>Pin</th>
<th>Function</th>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>AC Neutral</td>
<td>E</td>
<td>NA</td>
<td>I</td>
<td>NA</td>
</tr>
<tr>
<td>B</td>
<td>NA</td>
<td>F</td>
<td>Fault Monitor</td>
<td>J</td>
<td>NA</td>
</tr>
<tr>
<td>C</td>
<td>AC Line</td>
<td>G</td>
<td>DCG #2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>NA</td>
<td>H</td>
<td>EG (Equip Ground)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## CONNECTOR C15S:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Function</th>
<th>Pin</th>
<th>Function</th>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SP3TXD+</td>
<td>6</td>
<td>DCG #2</td>
<td>11</td>
<td>SP3TXC-</td>
</tr>
<tr>
<td>2</td>
<td>DCG #2</td>
<td>7</td>
<td>SP3RXC+</td>
<td>12</td>
<td>EG (Equip Ground)</td>
</tr>
<tr>
<td>3</td>
<td>SP3TXC+</td>
<td>8</td>
<td>DCG #2</td>
<td>13</td>
<td>SP3RXD-</td>
</tr>
<tr>
<td>4</td>
<td>DCG #2</td>
<td>9</td>
<td>SP3TXD-</td>
<td>14</td>
<td>NA</td>
</tr>
<tr>
<td>5</td>
<td>SP3RXD+</td>
<td>10</td>
<td>Port 1 Disable</td>
<td>15</td>
<td>SP3RXC-</td>
</tr>
</tbody>
</table>

### 3.18.8 Serial Port 3

Serial Port 3 shall control the TS 2 BIU Units using SDLC Protocol that meets the NEMA TS 2 Type 1 Frame Command / Response Standards. SP3DCD shall be allocated to Port 1 Disable where 0 VDC input on C15S pin 10 equals DCD inactive (False). SP3DCD shall be opto-isolated from Port 1 Disable.
3.19 4N (A) Power Supply Module

3.19.1 2070-4N Power Supply Module

The 2070-4N Power Supply Module supports the NEMA TS 1 and TS 2 Standards. The module is identical to the 2070-4A Power Supply Requirements except for the following:

- The power cord shall have a 15 inch ± 1 inch length as measured from the panel to the plug tips.
- The AC Power Fail voltage shall be 85VAC ±2VAC.
- The AC Power Restore voltage shall be 90VAC ±2VAC.
- The 2070-4N (A) power supply shall have proper marking Example “2070 4N (A)”. A permanent sticker shall be an acceptable marking method.
3.20 Model 2070-8 Field I/O Module

3.20.1 Module Consisting

The Module shall consist of the Module Chassis, Module Power Supply, FCU Controller, Parallel Input/Output Ports, Serial Communications Circuits and Module Connectors. The Module CHASSIS shall be made of 0.06 in. minimum aluminum sheet and treated with clear chromate. All external screws, except where called out, shall be countersunk and shall be Phillips flat head stainless steel. The matching nuts shall be permanently captive on the mating surfaces.

3.20.2 Module Front Panel

The Module Front Panel shall be furnished with the following:

1. ON/OFF POWER Switch mounted vertically with ON in the UP position.
2. LED DC Power Indicator. The indicator shall indicate that the required +5 VDC is within 3% and the +24 VDC is within 8%.
3. Incoming VAC fuse protection.
4. Two DB-25S COMM connectors labeled "EX1" & "EX2."
5. Four NEMA Connectors A, B, C, & D.

3.20.3 Label

A permanent Label shall be affixed to the Front Panel. The label shall display the unit's serial number. The number shall be permanent and easy to read.

3.20.4 Module Power Supply

A Module Power Supply shall be provided and located on the right side of the module as viewed from the front. The supply shall provide the necessary module internal circuitry DC power plus 2.0 Amperes minimum of +24 VDC for external logic, detector inputs, and output load control. The supply shall meet the following requirements:

3.20.4.1 Input Protection

Specification 3.12.3 Input Protection

3.20.4.2 Power Supply Requirements

The Power Supply shall meet the specification as listed in Section 3.12.6 Power Supply Requirements.

3.20.4.3 Tolerances

DC Voltage tolerances shall be ±3% for 5 VDC and ±8% for 24 VDC.

3.20.5 Incoming AC Power

The supplied Incoming AC Power shall be derived from Connector A Pins "p" (AC+) and "U" (AC Neutral). External +24 VDC shall be at Connector A, Pin "B" and Connector D Pin "NN." AC Power for the 2070 receptacle shall be tapped off from the secondary side of the ON Switch / Fuse configuration.
3.20.6 Module PC Boards

All Module PC Boards shall be mounted vertically.

3.20.7 POWERDOWN, NRESET, and LINESYNC

POWERDOWN, NRESET, and LINESYNC are incoming EIA-485 differential signals and shall be routed to the module via C12S Connector. The state of the module output ports at the time of POWERDOWN transition to LOW State and until NRESET goes HIGH shall be an open circuit.

3.20.8 Requirements

The Module shall meet all requirements under Section 3.10 Model 2070-2 Field I/O Module (F/I/O) with the following exceptions:

3.20.8.1 Parallel Ports

118 Bits of Input and 102 bits of Output shall be provided. Specification for inputs applies except the voltage is +24 in lieu of +12, Ground False ("0") exceeds 16.0 VDC, and Ground True ("1") is less than 8.0 VDC.

3.20.8.2 Serial Communication Circuitry

The module shall interface with the 2070-2B Field I/O module via HAR 1 Harness meeting EIA-485 Requirements. HAR 1 Harness shall be 23 lines minimum with a C12P Connector on one end and soldered with strain relief on the other. In addition to SP5 being routed to the FCU Controller interface, the SP3 EIA-485 Signal lines shall be routed only to the EX1 Connector.

3.20.9 EIA-232 Serial Port

An EIA-232 Serial Port on the FCU shall be provided with baud rate selection by Shunt of 0.3, 1.2, 2.4, 4.8, 9.6, 19.2, & 38.4 kbps asynchronous and shall be connected at EX1 Connector. This hardware is provided for future expansion capability and its use/protocol is currently undefined.

3.20.10 HAR 2 Harness

A 22-line minimum HAR 2 Harness shall be provided between EX2 Connector and Model 2070-6 Serial COMM Module in the 2070 UNIT. This provides two Modems or EIA-232 Interfaces between the 2070 UNIT and the outside world. The two EG (Equipment Ground) lines within HAR 2 shall be connected between EX2 and the 2070-8 module chassis.

3.20.11 Fault and Voltage Monitor Circuitry

NEMA TS 1 Controller Fault and Voltage Monitor functions (outputs to cabinet monitor) shall be provided.

3.20.11.1 OR Gates

Conceptually, two 3-input OR gates shall be provided. The gate 1 output shall be connected to Connector A, Pin A (Fault Monitor) and gate 2 output shall be connected to Connector A, Pin C. Any False state input shall cause a gate output False (+24VDC) state.

3.20.11.2 FCU Output O78

The FCU output O78 shall normally change its state every 100 ms. A module Watchdog circuit shall monitor the output. No state change for 2 ±0.1 seconds shall cause the circuit output to generate a
FALSE (+24 VDC) output (input to gates 1 and 2). Should the FCU begin changing state, the Watchdog output shall return to TRUE (0 VDC) state.

### 3.20.11.3 Operation

The module shall have a +5 VDC monitoring circuit which monitors the module’s +5 VDC (±0.25). If the voltage exceeds the limits, the circuit output shall generate a False output (input to gates 1 and 2). Normal operation shall return the output state to TRUE state.

### 3.20.11.4 Microprocessor Output

The FCU microprocessor output shall be assigned to FAULT Monitor (input to gate 1) and another output shall be assigned to VOLTAGE Monitor (input to gate 2).

### 3.20.11.5 Message Outputs

CPU Port 5 Set Output Command Message Outputs O78 and O79 shall be assigned to FAULT (O78) and VOLTAGE (O79). The bit logic state “1” shall be FCU output FALSE.

### 3.20.11.6 CPU / FCU Operations

CPU / FCU operation at POWER UP shall be as follows:

1. FCU Comm Loss Flag set. FAULT and VOLTAGE MONITOR outputs set to FALSE state.
2. CPU REQUEST MODULE STATUS COMMAND Message with “E” bit set is sent to FCU to clear Comm Loss Flag and FCU responds to CPU with “E” bit reset.
3. Before the Comm Loss timer expires, the SET OUTPUT COMMAND data must be sent. In that data, the 078 and 079 logically set to “0” will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted at the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.
4. * If the above message sequence is not followed, Comm Loss Flag shall be set (or remain) and VM & FM shall retain the FALSE output state.
5. Performs items 2 & 3 above User Software.

### 3.20.11.7 CPU / FCU Communications

A CPU / FCU Communications Loss during normal operation shall cause all outputs to go blank (FALSE state) and shall set the Comm. Loss Flag. FM and VM outputs shall be in FALSE state.
APPENDIX A – SECTION DETAILS

The detailed drawings found in this appendix contain a “Caltrans-style” information block (see Figure A-1). It has been left there to preserve uniformity with the Caltrans TEES 2009 and associated errata. It is not otherwise referenced or used by this standard.

<table>
<thead>
<tr>
<th>TITLE</th>
<th>MODEL 2070-CHASSIS</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>FRONT VIEW</td>
</tr>
<tr>
<td>NO SCALE</td>
<td>A9-1</td>
</tr>
<tr>
<td>TEES 2009</td>
<td></td>
</tr>
</tbody>
</table>

Figure A-1. Example Caltrans-style title block not used as part of this standard.
Figure A-2. Model 2070 – Chassis Front View.

NOTES: (FOR THIS DETAIL)

1. The unit shall be capable of mounting to a Standard 310B Rack using 4U open end mounting slots.
2. Continuous stainless steel hinge (0.157in maximum hinge barrel) that attaches to the Front Panel by two TSD #1 Thumb screw devices.
3. Actual location of ACTIVE light, AUX switch, CS0S, CS0J and contrast control shall be limited to ACTIVE light on the left side of the panel; AUX switch, CS0S, CS0J and the contrast control on the right side. They shall be located greater than 1 in from the edge of each other, other devices, connector or latch. CS0J only needs to be 0.25 in minimum from CS0S.
4. The length of the Front Panel Harness shall be 51n + 2% and it shall be removable.
5. LED indicators for each DC voltage shall be provided.
6. With the hinge installed, the distance between the TSD hole center and the CHASSIS Right Side (inside plane) shall be 0.55 in.
7. All dimensions shown are in inches.
Figure A-3. Model 2070 – Chassis Rear View.

NOTES: (FOR THIS DETAIL)

1. Four permanently attached 8 in long Card Guides SAE 1800F (OR EQUAL) beginning 0.51 in from the backplane mounting surface.
2. TB — TRANSITION BOARD
3. Maximum length of harness shall be 4 in, and shall not protrude beyond the back of the 2070 unit.
4. The VME Cage Assembly Opanning shall be delivered covered by a blank panel. Matching M3 PEM fasteners shall be provided on the back plane surface for panel mounting.
5. Blank plates shall cover all unused module openings.
6. All Module Front Plates thickness shall be (0.084±0.005)
7. All dimensions shown are in inches.
Figure A-4. Model 2070 – Chassis Top View.
Figure A-5. Model 2070 – Chassis Motherboard.
### Figure A-6. Model 2070 – Motherboard A1-A5 Connector Pinouts.

<table>
<thead>
<tr>
<th>A1 CONNECTOR PIN OUT</th>
<th>A2 TO A5 CONNECTOR PIN OUT</th>
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</thead>
<tbody>
<tr>
<td>PIN</td>
<td>A</td>
</tr>
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<td>1</td>
<td>SP1VD+</td>
</tr>
<tr>
<td>2</td>
<td>SP1X-</td>
</tr>
<tr>
<td>3</td>
<td>SP1GD+</td>
</tr>
<tr>
<td>4</td>
<td>SP1GD+</td>
</tr>
<tr>
<td>5</td>
<td>SP1GD+</td>
</tr>
<tr>
<td>6</td>
<td>SP1GD+</td>
</tr>
<tr>
<td>7</td>
<td>SP1GD+</td>
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<td>SP1GD+</td>
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<td>SP1GD+</td>
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<td>13</td>
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<td>14</td>
<td>SP1GD+</td>
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<td>16</td>
<td>NA</td>
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<td>NA</td>
</tr>
<tr>
<td>21</td>
<td>NCG M1</td>
</tr>
<tr>
<td>22</td>
<td>NMP (TX+)</td>
</tr>
<tr>
<td>23</td>
<td>NMP (TX-)</td>
</tr>
<tr>
<td>24</td>
<td>NA</td>
</tr>
<tr>
<td>25</td>
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<td>27</td>
<td>NCG M1</td>
</tr>
<tr>
<td>28</td>
<td>+12 VDC SER</td>
</tr>
<tr>
<td>29</td>
<td>+12 VDC</td>
</tr>
<tr>
<td>30</td>
<td>+12 VDC</td>
</tr>
<tr>
<td>31</td>
<td>ISO +12 VDC</td>
</tr>
<tr>
<td>32</td>
<td>ISO +12 VDC</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Functions are referenced to the CPU.
2. DCG #1 for +5VDC and +/-12VDC SER.
3. DCG #2 for ISO +12 VDC.
4. Connector A2 to A4, pins B21 and B22 shall read "NA".
   Connector A2, pins B23 shall read "A2 Installed".
   Connector A3, pins B23 shall read "A3 Installed".
   Connector A4, pins B23 shall read "NA".
   Connector A5, pins B21 shall read "A2 Installed".
   Connector A5, pins B22 shall read "DCG #1".
   Connector A5, pins B23 shall read "A3 Installed".
5. Pin A24 (NA) is reserved for network protection only, i.e., "Ethernet Shield".
6. Module installed in slot A2 enables SP1 & SP2 on 2070-1x modules.
7. Module installed in slot A3 enables SP5, on 2070-1x modules.
8. SP3 and SP5 are always enabled.
9. "C50 ENABLE" Active (e.g. DCG #1) is used by module installed in slot A1 to disable its channel 2 (i.e. SP4).
10. NetP6 signals TX+, TX-, RX+, RX- respectively.

<table>
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<tr>
<td>MODEL 2070-MOTHERBOARD A1-A5 CONNECTOR PIN OUT</td>
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<th>NS SCALE</th>
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</tr>
</thead>
<tbody>
<tr>
<td>TEEC 2009</td>
<td></td>
</tr>
</tbody>
</table>
Figure A-7. Model 2070 – System PCB Modules, General.

NOTES: (FOR THIS DETAIL)

1. All Thumb-screw devices on modules described in this drawing shall be TSD#3 or equal.
2. 96 pin DIN connector
   ELCO # 00 5272 98 000 D13 or equal.
3. All dimensions shown are in inches.
Figure A-8. Model 2070-1E CPU Modules & Serial Port/SDLC Protocol.
**Figure A-9. Model 2070-2 Field I/O Modules.**

**NOTES: (FOR THIS DETAIL)**

1. 2070-2E Faceplate shall be 4X wide. 2070-2C Faceplate shall be 2X wide.  
   (SEE SYSTEM PCB MODULE, GENERAL DETAILS.)

2. Dark Grommet in the C1S Connector denote guide pin locations and open circles denote guide socket locations.

3. Dimension "A" shall be a minimum of 0.5in.

4. C1S - M104 Type, C1IS - 37-Pin Circular Plastic Type.

5. C12S - 25-Pin DB Socket Type
   C12S pin 12 (BIAS +5VDC) at 50mA maximum is derived from the ISO +12 VDC Power Supply.  
   BIAS +5VDC refers to voltage required for a Line Terminator device.

6. EG (Equipment Ground) pin is electrically connected to the faceplate.

7. LED indicators Tx & Rx for SP3 (field site) and SP5 shall be provided.

8. C1 connector shall be bolted to the front plate.

**TABLE:**

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<th>TITLE:</th>
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### CIS PIN ASSIGNMENT

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<th>PIN</th>
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<th>NAME</th>
<th>PIN</th>
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<td>DCG #2</td>
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Figure A-10. Model 2070-2A Field I/O Module, C1 & C11 Connectors.
Figure A-11. Model 2070-3A, 3B & 3D Front Panel Assemblies.

NOTES: (FOR THIS DETAIL)

1. Key size shall be (0.030±0.005) in.
2. Key center to center spacing shall be 0.50 in.
3. Edge slot shall be a 0.060-0.060 in square.
4. The 40 contact connector shall be similar to AMP 103143-8 or equal & compatible to the FF harness type and pin assignments.
5. Center of the FF harness connector shall be vertically positioned (0.44±0.127) in measured from the top of the FPA.
6. The connector shall be a right angle connector with pin 1 located on the lower right hand corner.
7. Two position LOGIC switch mounted vertically.
8. "CS60" connector shall be a 0.90 in dia. contact connector. "CS60" shall be a RI-45 9-position jack.
9. "CRP" connector shall be a DE-6 plug contact connector.
10. Front panel sheet metal thickness shall be (0.060±0.005) in.
11. The FPA shall be provided with a continuous top and bottom 0.030 (inside dimension) 1/8 in. dimension to the front panel and extend the full length of the FPA.
12. CS6P B Box Power is T-500C, 120VAC max. All signals on CS6P are referenced to isolated interface ground (DGND).
### Model 2070-3 AUX Switch Codes

<table>
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<th>Switch Position</th>
<th>ASCII Data (Text)</th>
<th>ASCII Data (HEX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td>ESC O T</td>
<td>1B 4F 54</td>
</tr>
<tr>
<td>OFF</td>
<td>ESC O U</td>
<td>1B 4F 55</td>
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</table>

### Model 2070-3 Key Codes

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<th>ASCII Data (Text)</th>
<th>ASCII Data (HEX)</th>
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<tr>
<td>E</td>
<td></td>
<td>45</td>
</tr>
<tr>
<td>F</td>
<td></td>
<td>46</td>
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<tr>
<td>(UP ARROW)</td>
<td>ESC [ A</td>
<td>1B 5B 41</td>
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<tr>
<td>(DOWN ARROW)</td>
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<td>1B 5B 42</td>
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<td>ENTER</td>
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**Figure A-12. Model 2070-3 FPA Key Codes.**
### Configuration Command Codes

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<th>HEX Value</th>
<th>Function</th>
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<td>N1</td>
<td>B9</td>
<td>Move cursor to next tab stop</td>
</tr>
<tr>
<td>R0</td>
<td>80</td>
<td>Position cursor at first position on current line</td>
</tr>
<tr>
<td>LF</td>
<td>1A</td>
<td>Line Feed / Move cursor down one line</td>
</tr>
<tr>
<td>BS</td>
<td>08</td>
<td>Backspace / Move cursor one position to the left and write space</td>
</tr>
<tr>
<td>ESC C P1 P2 F</td>
<td>1B 43 66</td>
<td>Position cursor at current position</td>
</tr>
<tr>
<td>ESC C Pn R</td>
<td>1B 3B Pn 42</td>
<td>Position cursor Pn positions right</td>
</tr>
<tr>
<td>ESC C Pn L</td>
<td>1B 3B Pn 41</td>
<td>Position cursor Pn positions left</td>
</tr>
<tr>
<td>ESC C Pn D</td>
<td>1B 3B Pn 44</td>
<td>Position cursor Pn positions down</td>
</tr>
<tr>
<td>ESC C Pn U</td>
<td>1B 3B Pn 45</td>
<td>Position cursor Pn positions up</td>
</tr>
<tr>
<td>ESC C 6 J</td>
<td>1B 3B 32 44</td>
<td>Clear screen with spaces without moving cursor</td>
</tr>
<tr>
<td>ESC C</td>
<td>1B 62</td>
<td>Soft reset</td>
</tr>
<tr>
<td>ESC F P1 (Pn 1) PnD</td>
<td>1B 3B P1 SB Pn SB Pn 66</td>
<td>Clear special character number Pn (1-8) at current cursor position</td>
</tr>
<tr>
<td>ESC C Pn V</td>
<td>1B 3B Pn 56</td>
<td>Display special character number Pn (1-8) at current cursor position</td>
</tr>
<tr>
<td>ESC C 25 h</td>
<td>1B 32 25 48</td>
<td>Turn character blink on</td>
</tr>
<tr>
<td>ESC C 25 l</td>
<td>1B 32 25 60</td>
<td>Turn character blink off</td>
</tr>
<tr>
<td>ESC C 5 h</td>
<td>1B 3B 50 68</td>
<td>Blinkmate background</td>
</tr>
<tr>
<td>ESC C 5 l</td>
<td>1B 3B 50 68</td>
<td>Blinkmate background off</td>
</tr>
<tr>
<td>ESC C 33 l</td>
<td>1B 3B 33 60</td>
<td>Cursor blink off</td>
</tr>
<tr>
<td>ESC C 33 h</td>
<td>1B 3B 33 60</td>
<td>Cursor blink on</td>
</tr>
<tr>
<td>ESC C 37 h</td>
<td>1B 3B 37 68</td>
<td>Reverse Video on -Note 2</td>
</tr>
<tr>
<td>ESC C 37 l</td>
<td>1B 3B 37 68</td>
<td>Reverse Video off -Note 2</td>
</tr>
<tr>
<td>ESC C 24 k</td>
<td>1B 3B 24 68</td>
<td>Underline on -Note 2</td>
</tr>
<tr>
<td>ESC C 24 l</td>
<td>1B 3B 24 68</td>
<td>Underline off -Note 2</td>
</tr>
<tr>
<td>ESC C 6 n</td>
<td>1B 3B 30 60</td>
<td>All attributes off</td>
</tr>
<tr>
<td>ESC C</td>
<td>1B 40</td>
<td>Set tab stop at current cursor position</td>
</tr>
<tr>
<td>ESC C Pn g</td>
<td>1B 3B Pn 67</td>
<td>Pn = 0 : Clear Tab at Current Position, Pn = 1 to 8 : Clear All Tabs</td>
</tr>
<tr>
<td>ESC C 17 h</td>
<td>1B 3B 17 68</td>
<td>Auto-wrap on</td>
</tr>
<tr>
<td>ESC C 17 l</td>
<td>1B 3B 17 68</td>
<td>Auto-wrap off</td>
</tr>
<tr>
<td>ESC C 16 h</td>
<td>1B 3B 16 68</td>
<td>Auto-repeat on</td>
</tr>
<tr>
<td>ESC C 16 l</td>
<td>1B 3B 16 68</td>
<td>Auto-repeat off</td>
</tr>
<tr>
<td>ESC C 15 h</td>
<td>1B 3B 15 60</td>
<td>Cursor off</td>
</tr>
<tr>
<td>ESC C 15 l</td>
<td>1B 3B 15 60</td>
<td>Cursor on</td>
</tr>
<tr>
<td>ESC C 47 h</td>
<td>1B 3B 47 68</td>
<td>Auto-scroll on</td>
</tr>
<tr>
<td>ESC C 47 l</td>
<td>1B 3B 47 68</td>
<td>Auto-scroll off</td>
</tr>
<tr>
<td>ESC C 41 R</td>
<td>1B 3B 41 68</td>
<td>Set backlight brightness value to Pn (0-63)</td>
</tr>
<tr>
<td>ESC C P0</td>
<td>1B 3B 35</td>
<td>String sent to CPU when FPA power up</td>
</tr>
</tbody>
</table>

**Notes:**

1. Numerical values have one ASCII character per digit without leading zeros.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A 3B & 3D.
   Command codes shall be available for Option 3C (C60P).

### Inquiry Command-Response Codes

<table>
<thead>
<tr>
<th>Command</th>
<th>Response</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Module to Front Panel Module</td>
<td>Front Panel Module to CPU Module</td>
<td>Inquiry Cursor Position</td>
</tr>
<tr>
<td>ESC C 6 n</td>
<td>ESC (Pn Pk R)</td>
<td>1B 3B Pk 50 Pk 55</td>
</tr>
<tr>
<td>ESC C 6 n</td>
<td>ESC (PnPnPkn Pk R)</td>
<td>1B 3B Pk 50 Pk 55</td>
</tr>
<tr>
<td>ESC C 6 n</td>
<td>ESC (PnPnPkn Pk R)</td>
<td>1B 3B Pk 50 Pk 55</td>
</tr>
<tr>
<td>ESC C 6 n</td>
<td>ESC (PnPnPkn Pk R)</td>
<td>1B 3B Pk 50 Pk 55</td>
</tr>
<tr>
<td>ESC C 6 n</td>
<td>ESC (PnPnPkn Pk R)</td>
<td>1B 3B Pk 50 Pk 55</td>
</tr>
<tr>
<td>ESC C 6 n</td>
<td>ESC (PnPnPkn Pk R)</td>
<td>1B 3B Pk 50 Pk 55</td>
</tr>
</tbody>
</table>

---

**Figure A-13. Model 2070-3 FPA Display Codes.**
Figure A-14. Model 2070-4 Power Supply Module.
Figure A-15. Model 2070-5 VME Cage Assembly.

NOTES: (FOR THIS DETAIL)

1. PS1 Harness Interfaces between the Model 2070-4 Power Supply Module and the 2070-8 VME Cage Assembly. The harness shall be permanently attached to the Cage Assembly by solder, FastOn or Power Bugs. The Harness wiring shall be 8 #18 conductors for power and 2 #22 conductors for others.

2. The plate shall cover the open area & attach to the Chassis Backplane mounting surface via 16 #3 thumbcrews. The screws shall mate with the PEM nuts as specified in the Model 2070 Chassis Top View Detail.

3. 6-32 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the 6-32 screws on the top and bottom of the Model 2070 chassis.

4. All dimensions shown are in inches.

---

**PS1 CONNECTOR PIN ASSIGNMENT**

<table>
<thead>
<tr>
<th>PIN</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>2</td>
<td>+12 VDC SER</td>
</tr>
<tr>
<td>3</td>
<td>-12 VDC SER</td>
</tr>
<tr>
<td>4</td>
<td>DIG #1 (+5 VDC &amp; +12 SER)</td>
</tr>
<tr>
<td>5</td>
<td>+5 VDC Standby</td>
</tr>
<tr>
<td>6</td>
<td>+5 VDC Sense</td>
</tr>
<tr>
<td>7</td>
<td>DIG #1 Sense</td>
</tr>
<tr>
<td>8</td>
<td>AC FAIL</td>
</tr>
<tr>
<td>9</td>
<td>SIGRESET</td>
</tr>
<tr>
<td>10</td>
<td>NA</td>
</tr>
</tbody>
</table>

---

**TABLE: MODEL 2070-5 VME CAGE ASSEMBLY**

| HD SCALE | TEES 2009 | A9-14 |
### SERIAL PORT DESCRIPTORS DEFAULTS

<table>
<thead>
<tr>
<th>SP1, SP2, SP3 and SP5</th>
<th>SP4</th>
<th>SP5</th>
<th>SP6</th>
</tr>
</thead>
<tbody>
<tr>
<td>noeupc</td>
<td>noeupc</td>
<td>noeupc</td>
<td>noeupc</td>
</tr>
<tr>
<td>bab</td>
<td>bab</td>
<td>bab</td>
<td>bab</td>
</tr>
<tr>
<td>bel</td>
<td>bel</td>
<td>bel</td>
<td>bel</td>
</tr>
<tr>
<td>noecho</td>
<td>echo</td>
<td>echo</td>
<td>noecho</td>
</tr>
<tr>
<td>if</td>
<td>if</td>
<td>if</td>
<td>if</td>
</tr>
<tr>
<td>null=0</td>
<td>null=0</td>
<td>null=0</td>
<td>null=0</td>
</tr>
<tr>
<td>nopause</td>
<td>nopause</td>
<td>nopause</td>
<td>nopause</td>
</tr>
<tr>
<td>pag=24</td>
<td>pag=24</td>
<td>pag=24</td>
<td>pag=24</td>
</tr>
<tr>
<td>bsp=08</td>
<td>bsp=08</td>
<td>bsp=08</td>
<td>bsp=08</td>
</tr>
<tr>
<td>def=16</td>
<td>def=16</td>
<td>def=16</td>
<td>def=16</td>
</tr>
<tr>
<td>eor=0D</td>
<td>eor=0D</td>
<td>eor=0D</td>
<td>eor=0D</td>
</tr>
<tr>
<td>eot=18</td>
<td>eot=18</td>
<td>eot=18</td>
<td>eot=18</td>
</tr>
<tr>
<td>reprint=04</td>
<td>reprint=04</td>
<td>reprint=04</td>
<td>reprint=04</td>
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<td>dup=01</td>
<td>dup=01</td>
<td>dup=01</td>
<td>dup=01</td>
</tr>
<tr>
<td>pac=17</td>
<td>pac=17</td>
<td>pac=17</td>
<td>pac=17</td>
</tr>
<tr>
<td>abort=03</td>
<td>abort=03</td>
<td>abort=03</td>
<td>abort=03</td>
</tr>
<tr>
<td>quit=05</td>
<td>quit=05</td>
<td>quit=05</td>
<td>quit=05</td>
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<tr>
<td>bs=08</td>
<td>bs=08</td>
<td>bs=08</td>
<td>bs=08</td>
</tr>
<tr>
<td>bel=07</td>
<td>bel=07</td>
<td>bel=07</td>
<td>bel=07</td>
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<td>type=00</td>
<td>type=00</td>
<td>type=00</td>
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<td>baud=1200</td>
<td>baud=9600</td>
<td>baud=38400</td>
<td>baud=9600</td>
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<td>xon=11</td>
<td>xon=00</td>
<td>xon=11</td>
<td>xon=11</td>
</tr>
<tr>
<td>xoff=13</td>
<td>xoff=00</td>
<td>xoff=13</td>
<td>xoff=13</td>
</tr>
<tr>
<td>tabs=09</td>
<td>tabs=09</td>
<td>tabs=09</td>
<td>tabs=09</td>
</tr>
<tr>
<td>tabs=4</td>
<td>tabs=4</td>
<td>tabs=04</td>
<td>tabs=04</td>
</tr>
</tbody>
</table>

**NOTES:** (FOR THIS DETAIL)

1. All serial port descriptors shall be set with 8 Bit Word, 1 Stop & no Parity.
2. Model 2070-1C sp4 shall be set to 38.4 Kbps.
3. sp3s & sp5s shall be set to 614.4 Kbps.

### Figure A-16. Model 2070 – Serial Port Descriptors Defaults.
Figure A-17. Model 2070 – Power Failure Reaction.
Figure A-18. Model 2070-6 ASYNC-Modem Serial Comm Module.
Figure A-19. Model 2070-7 ASYNC Serial Comm Module.
Figure A-20. Model 2070-9D Dial-Up Modem Comm Module.
NOTES: (FOR THIS DETAIL)

1. The Model 2070 Controller Unit is shown only for reference.
2. The bottom supports shall be double flanged.
3. A = Connector A (MS-3112-22-55P Type)
   B = Connector B (MS-3112-22-SSS Type)
   C = Connector C (MS-3112-24-61S Type)
   D = Connector D (MS-3112-24-61P Type)
   EX1 = Connector EX1 (DB-25P Type)
   EX2 = Connector EX2 (DB-25S Type)
4. All dimensions shown are in inches.

Figure A-21. Model 2070E N1 Front View.
Figure A-22. Model 2070E N1 Side View.
Figure A-23. Model 2070-8 ISO View.

NOTES: (FOR THIS DETAIL)
1. The module housing bottom shall be slat vented. The top shall be open.
2. All dimensions shown are in inches.
### Figure A-24. Model 2070-8 Field I/O Module, Connector A & B.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Connector A</th>
<th>Connector B</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Fault Monitor</td>
<td>Phase 1 Next</td>
</tr>
<tr>
<td>B</td>
<td>---</td>
<td>Reserved</td>
</tr>
<tr>
<td>C</td>
<td>Voltage Monitor</td>
<td>Phase 2 Next</td>
</tr>
<tr>
<td>D</td>
<td>Phase 1 Red</td>
<td>Phase 3 Green</td>
</tr>
<tr>
<td>E</td>
<td>Phase 1 Don't Walk</td>
<td>Phase 3 Yellow</td>
</tr>
<tr>
<td>F</td>
<td>Phase 2 Red</td>
<td>Phase 3 Red</td>
</tr>
<tr>
<td>G</td>
<td>Phase 2 Don't Walk</td>
<td>Phase 4 Red</td>
</tr>
<tr>
<td>H</td>
<td>Phase 2 Flasher</td>
<td>Phase 4 Flasher</td>
</tr>
<tr>
<td>J</td>
<td>Phase 2 Flasher</td>
<td>Phase 4 Don't Walk</td>
</tr>
<tr>
<td>K</td>
<td>Phase 2 Vehicle Detector</td>
<td>Phase 4 Vehicle Detector</td>
</tr>
<tr>
<td>L</td>
<td>Phase 3 Pedestrian Detector</td>
<td>Phase 4 Vehicle Detector</td>
</tr>
<tr>
<td>M</td>
<td>Phase 1 Hold</td>
<td>Phase 4 Pedestrian Detector</td>
</tr>
<tr>
<td>N</td>
<td>Stop Time (Ring D)</td>
<td>Phase 3 Vehicle Detector</td>
</tr>
<tr>
<td>P</td>
<td>Inh Max Term (Ring D)</td>
<td>Phase 3 Pedestrian Detector</td>
</tr>
<tr>
<td>Q</td>
<td>External Start</td>
<td>Phase 3 Unit</td>
</tr>
<tr>
<td>R</td>
<td>Internal Advance</td>
<td>Phase 2 Unit</td>
</tr>
<tr>
<td>S</td>
<td>Phase 2 Flasher</td>
<td>Phase 4 Unit</td>
</tr>
<tr>
<td>T</td>
<td>Indication Lamp Control</td>
<td>Phase 4 Ped Uni</td>
</tr>
<tr>
<td>U</td>
<td>Phase 1 Unit</td>
<td>Phase 4 D</td>
</tr>
<tr>
<td>V</td>
<td>Phase 1 Pedestrian Detector</td>
<td>Phase 4 Unit</td>
</tr>
<tr>
<td>W</td>
<td>Phase 1 Hold</td>
<td>Phase 4 Unit</td>
</tr>
<tr>
<td>X</td>
<td>Phase 1 Hold</td>
<td>Phase 4 Unit</td>
</tr>
<tr>
<td>Y</td>
<td>Phase 1 Hold</td>
<td>Phase 4 Unit</td>
</tr>
<tr>
<td>Z</td>
<td>Phase 1 Hold</td>
<td>Phase 4 Unit</td>
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**Title:** 2070-B FILED I/O MODULE CONECTOR A & B

**No Scale:**  A11-4

**Tees:** 2009
<table>
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<tr>
<td><strong>PIN</strong></td>
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<tr>
<td>A</td>
<td>Cooked Status Bit A (Ring 2)</td>
</tr>
<tr>
<td>B</td>
<td>Cooked Status Bit B (Ring 2)</td>
</tr>
<tr>
<td>C</td>
<td>Phase 8 Don’t Walk</td>
</tr>
<tr>
<td>D</td>
<td>Phase 7 Red</td>
</tr>
<tr>
<td>E</td>
<td>Phase 7 Yellow</td>
</tr>
<tr>
<td>F</td>
<td>Phase 7 Red</td>
</tr>
<tr>
<td>G</td>
<td>Phase 7 Red</td>
</tr>
<tr>
<td>H</td>
<td>Phase 7 Red</td>
</tr>
<tr>
<td>I</td>
<td>Phase 7 Yellow</td>
</tr>
<tr>
<td>J</td>
<td>Phase 7 Red</td>
</tr>
<tr>
<td>K</td>
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</tr>
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<td>L</td>
<td>Phase 7 Don’t Walk</td>
</tr>
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<td>M</td>
<td>Phase 8 Next</td>
</tr>
<tr>
<td>N</td>
<td>Phase 8 Off</td>
</tr>
<tr>
<td>P</td>
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</tr>
<tr>
<td>Q</td>
<td>Phase 8 Pedestrian Detector</td>
</tr>
<tr>
<td>R</td>
<td>Phase 8 Pedestrian Detector</td>
</tr>
<tr>
<td>S</td>
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</tr>
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<td>T</td>
<td>Phase 7 Pedestrian Detector</td>
</tr>
<tr>
<td>U</td>
<td>Phase 7 Pedestrian Detector</td>
</tr>
<tr>
<td>V</td>
<td>Phase 7 Pedestrian Detector</td>
</tr>
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<td>W</td>
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<td>Phase 8 Pedestrian Detector</td>
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<tr>
<td>Y</td>
<td>Phase 8 Pedestrian Detector</td>
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<tr>
<td>Z</td>
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</tr>
<tr>
<td>b</td>
<td>Phase 8 Pedestrian Detector</td>
</tr>
<tr>
<td>c</td>
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<td>d</td>
<td>Phase 8 Pedestrian Detector</td>
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<td>e</td>
<td>Phase 8 Pedestrian Detector</td>
</tr>
<tr>
<td>f</td>
<td>Phase 8 Pedestrian Detector</td>
</tr>
<tr>
<td>g</td>
<td>Phase 8 Pedestrian Detector</td>
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<td>h</td>
<td>Phase 8 Pedestrian Detector</td>
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<tr>
<td>i</td>
<td>Phase 8 Pedestrian Detector</td>
</tr>
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<td>j</td>
<td>Phase 8 Pedestrian Detector</td>
</tr>
<tr>
<td>k</td>
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</tr>
<tr>
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<td>n</td>
<td>Phase 8 Pedestrian Detector</td>
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<td>Phase 8 Pedestrian Detector</td>
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<tr>
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<td>Phase 8 Pedestrian Detector</td>
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<td>s</td>
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<td>t</td>
<td>Phase 8 Pedestrian Detector</td>
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<td>u</td>
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<td>v</td>
<td>Phase 8 Pedestrian Detector</td>
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<tr>
<td>w</td>
<td>Phase 8 Pedestrian Detector</td>
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<td>x</td>
<td>Phase 8 Pedestrian Detector</td>
</tr>
<tr>
<td>y</td>
<td>Phase 8 Pedestrian Detector</td>
</tr>
<tr>
<td>z</td>
<td>Phase 8 Pedestrian Detector</td>
</tr>
<tr>
<td>AA</td>
<td>Phase 8 Pedestrian Detector</td>
</tr>
<tr>
<td>BB</td>
<td>Phase 8 Pedestrian Detector</td>
</tr>
<tr>
<td>CC</td>
<td>Phase 8 Pedestrian Detector</td>
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<td>DD</td>
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<td>PP</td>
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**Figure A-25. Model 2070-8 Field I/O Module, Connector C & D.**
### EX1 Connector Pinout

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</thead>
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<tr>
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<td>EQ GND</td>
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<tr>
<td>2</td>
<td>TXD (FCU)</td>
</tr>
<tr>
<td>3</td>
<td>RXD (FCU)</td>
</tr>
<tr>
<td>4</td>
<td>RTS (FCU)</td>
</tr>
<tr>
<td>5</td>
<td>CTS (FCU)</td>
</tr>
<tr>
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<td>NA</td>
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<tr>
<td>7</td>
<td>2070-8 I/O GND</td>
</tr>
<tr>
<td>8</td>
<td>IFC GND</td>
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### EX2 Connector Pinout

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<td>TXI (Channel 1)</td>
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<tr>
<td>3</td>
<td>RXI (Channel 1)</td>
</tr>
<tr>
<td>4</td>
<td>RTS (Channel 1)</td>
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<tr>
<td>5</td>
<td>CTS (Channel 1)</td>
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<tr>
<td>7</td>
<td>IFC GND</td>
</tr>
<tr>
<td>8</td>
<td>DCI (Channel 1)</td>
</tr>
<tr>
<td>9</td>
<td>AUDIO IN (Channel 1)</td>
</tr>
<tr>
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<td>AUDIO IN (Channel 1)</td>
</tr>
<tr>
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<td>AUDIO OUT (Channel 1)</td>
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<tr>
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<td>EQ (Equipment Ground)</td>
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<tr>
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**Figure A-26. Model 2070-8 Field I/O Module, EX1 & EX2 Connectors.**
Figure A-27. Model 2070-2N Field I/O Module.