

*Expedited Draft ATC Controller Standard
Changes from Rev 1.0.5 to Rev 2*

Significant changes in Revision 2, June 2003 (from Revision 1.0.5, April 2003) include:

GENERAL

- Name change from ATC-3000
 - *Recognizing the concerns of the user community, standard name is now ATC Controller*

PORTS

- Justification of Number and Functionality of Designated Ports
 - *Retained full complement of ports from previous draft, with justification*
 - *Provided option for minimal version of ATC, with non-functional ports terminated by manufacturer to allow future use*
 - *Added serial EEPROM to give port information at Host Board*
- Ethernet Ports
 - *Opted for second Ethernet port on Engine Board*
 - *Connection details outlined below*
- Location of Media Independent Interface (MII)
 - *Not required on Engine Board, but allowed as an option at user interface*

ENGINE BOARD

- Response to questions raised about Engine Board pin assignments
 - *Pin assignments unchanged after detailed engineering assessment*
 - *Interface restricted to logic signals only*
- Engine board connectors
 - *Unchanged after careful consideration of options*
- Reconsider Engine Board size to allow use on a 3U card
 - *Retained previously specified Engine Board size, with options*

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- Reexamine the Engine Board mounting height and overall envelope restrictions
 - *Revision 2 contains design revisions detailed in mechanical diagrams and accompanying text*
- Other Engine Board issues
 - *Proprietary interface programming and test port pins allowed on engine board with caveat regarding interchangeability of boards*
 - *Standby power sources unchanged*
 - *Parallel interface considered and rejected*
 - *Start-up time requirement rewritten*
 - *POWERUP and POWERDOWN signals detailed*
 - *SYSCLK_DIV_4 removed*
 - *More general designation of memory characteristics (e.g., FLASH)*

OTHER

- Response to questions raised about overall controller size
 - *Maximum vertical height remains at 7” but will defer to user comments*
- Performance benchmarks clarified
 - *Retain 200 MIPS using Dhrystone 2.1, with discussion*
- Response to questions raised about removable data memory
 - *DataKey remains best option based on user needs*
 - *Related control signals reconsidered in design*
- Extensive changes to environmental and testing details
 - *Selected details consistent with ATC cabinet standard*
- Inclusion of Performance and Material Requirements
- Inclusion of Quality Control section
- Revisions to Glossary

Details behind these decisions are given below:

GENERAL

Name change from ATC-3000 to ATC Controller

The original choice to call this standard ATC-3000 was intended to indicate how changes in software and hardware design philosophies influence the overall design specified in this controller standard. However, users indicated during the comment period that this name suggested a controller model superceding the 2070, which is pointedly not the intention of this work. Therefore, **the name of the standard is changed to the more generic ATC Controller** to reflect its intention to be inclusive of the 2070 and other controller designs.

PORTS

Justification of Number and Functionality of Designated Ports

Attendees at the previous review meeting in Houston asked that the number of required ports be justified in terms of required functionality and that sufficient flexibility be allowed for manufacturers to meet user needs (from minimal to normal to enhanced versions of an Engine Board, for example). There was a general agreement that at least one port should allow interrogation of the system to determine installed features.

Resolution

1. After careful consideration, the team decided that **all of the ports previously specified for the Engine Board will be retained** as discussed below. The Engine Board is required to provide the full complement of ports specified in Revision 2.
 - a. **A minimum set of ports, specified in Revision 2, must be terminated on the controller's external panel(s).**
 - b. **Manufacturers are free to select any or all of the remaining ports for external termination.**
2. **A serial EEPROM has been added to the Host Module to provide configuration information to the Engine Board regarding the specific port complement of the Host Module.**

Discussion/Explanation

The consultant team considered each of the intended uses of the ports specified previously in light of the user discussions at and subsequent to the draft review meeting held in Houston (April 2003). We agreed with the comments by several

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users in attendance at the meeting that each of the specified ports served a legitimate purpose, and that a reduction in number of ports would constitute a step backwards in design options.

As a compromise, the consultant team decided that minimal versions of the ATC could be built with fewer active ports than the maximum number required. Such an option would be considered consistent with the spirit of the ATC Controller standard as long as the each Engine Board is able to support the full complement of specified ports. In the interest of future compatibility and interoperability, the standard does not allow for a 'lite' Engine Board version. A careful examination of available microprocessors that would most likely be used for this purpose indicated that there was little (if any) additional cost (for users or manufacturers) associated with this decision because most of the ports were provided on-chip.

A serial EEPROM device is now required by the standard to provide information between Host and Engine Board about available ports. This EEPROM will be accessed using the serial port interface (SPI) port using a chip select dedicated to this purpose. The specific format of the configuration data is specified in Revision 2. Data retrieval from the EEPROM will be handled by the ATC API.

PORTS

Ethernet Ports

Users requested at least two distinct Ethernet ports and consideration of MII or RMII as the standard Ethernet interface.

Resolution

- 1. A second Ethernet port is added to the Engine Board.**
- 2. Both Engine Board Ethernet ports are 10Mb 10BASE-T and provide a twisted-pair interface at the Engine Board connector.**
- 3. MII is permitted as a hub-based Host Module feature, either to internal PHY devices or to an external MII40 connector.**
- 4. A second hub is added to the overall controller architecture to support the second Ethernet port.**

Discussion/Explanation

After considering the implications of a single Ethernet port, supported by a four-port hub from the Engine Board, it became apparent that network administration, security and network loading issues would be significantly simpler to manage if there were two distinct Ethernet ports on the Engine Board.

In addition to adding another Ethernet port to the Engine Board, another hub was added to the overall controller architecture. Each of these two hubs will separately support a distinct Engine Board Ethernet port and a minimum of two additional external connections.

The specific functionality of each Engine Board Ethernet port will not be dictated by this standard, but it is envisioned that one Ethernet port would support local (cabinet) device expansion, while the other Ethernet port would support remote (network) communications and local control interfaces.

As a functional requirement, the consultant team discussed the issue of Ethernet speed at length, considering both the anticipated needs and the extra costs associated with over-specification of speed. The consultant team could not determine any possible application in the foreseeable future which would require more than a 10Mb local or remote network interface into the Engine Board. Limiting the speed of both Ethernet ports to 10Mb simplifies the electrical interface to the Engine Board and improves the overall reliability of controller operation, as the CPU is not required to process network data at rates which could approach its own internal clock rate and thereby could introduce significant complexities in software design or architecture.

The consultant team also investigated the issue of MII/RMII and decided that MII is inappropriate at the Engine Board level (see also the next section of this synopsis) as both Ethernet ports are to be internally connected to hub ICs. However, using MII at the hub interface might provide flexibility with external media (PHY). A cursory investigation of suitable hub ICs was performed. Three- and five-port versions were found to be available with 10/100 auto negotiation, on-board switches, twisted-pair transceivers, frame buffering and available single MII interface for less than \$10 when purchased in quantity (see, for example, http://www.micrel.com/_PDF/Kendin/ks8993.pdf).

Hub ICs with host MII/RMII interfaces also require a repeater/switch ASIC or microprocessor which make the total cost per-hub considerably more expensive.

Location of Media Independent Interface (MII)

One commenter (Clyde Neel of Naztec) requested that MII replace the 10/100 Base T interface specified in the standard as part of the Engine Board. The reasons given were:

- Electrical performance – The MII is a logic signal interface designed for transmittal on a printed circuit board assembly. The physical driver device (electrical or optical) would be located on the host board. This allows it to be located physically next to the Ethernet connector on the edge of the board, which is the written recommendation of every device manufacturer surveyed. The MII achieves lower signal bandwidths by transferring data four bits at a time; data rates of 100 Mbps are achieved with signal rates of ¼ what would otherwise be required.
- Flexibility – The MII is an interface between the MAC controller and the physical driver (referred to as the PHY or PHYciever). The advantage to placing the interface here is that the MAC controller is located on the Engine board; this satisfies the desire to have the Ethernet software drivers determined by devices on the Engine Board. However, since the physical driver device is located on the host board, it is not limited to any particular type. Different electrical and even fiber optic media may be supported, which explains its name of Media Independent Interface.
- Reduced Obsolescence – The MII is an interface specified in the IEEE 802.3 Ethernet standard. It is supported by multiple manufacturers of Ethernet integrated circuits and is also found on communication microprocessors.

Upon careful consideration of these arguments, and good engineering practices, the consultant team recommends that **the Engine Board not be required to include an MII, but that an MII be allowed at the user interface (left to manufacturer and user**

discretion). This achieves the goal of flexibility in the interface while reducing the introduction of other problems on the Engine Board. Specifically:

- Electrical Performance: The statement “...*data rates of 100 Mbps are achieved with signal rates of 1/4...*” means that four 25 MHz signal return current loops are created. This is in direct conflict with a previous comment (also by Clyde Neel of Naztec) that high-frequency signal current loops should be avoided on the Engine Board. It is also in conflict with the MII standard, which requires a specific connector with high-speed signal return grounds on pins 22-39. The Draft Engine Board design has no high-speed signal current returns, as all signal current returns are low-speed, while each high-speed signal has a differential current return (see separate comment below regarding Engine Board pin assignments).
- Flexibility: “*Different electrical and even fiber optic media may be supported, which explains its name of Media Independent Interface.*” While this comment is technically correct, it does not apply to the Engine Board. The Engine Board attaches to the internal hub, not the cabinet (refer to the Block Diagram). An Engine Board MII connector would be inaccessible to the user.
- Reduced Obsolescence: The Naztec comment implies the Engine Board may become obsolete if it bans the use of MII chips. Exactly the opposite is true. This draft standard allows all technologies, including MII, at the user interface but sets guidelines on the Engine Board to allow this flexibility at the user interface. By contrast, the Naztec proposal would ban all technologies except MII on the Engine Board. To clarify:
 - This draft standard allows the use of an MII chip in a manner that does not affect the Host Board. One side of the MII chip connects to the microprocessor, while the other side of the MII chip connects to the Ethernet Transformer. If MII is replaced by another technology, this draft standard allows that new technology so long as it can be made to conform to the interfaces indicated in the standard.
 - The Naztec proposal would force the use of MII chips, and also require the MII signals be included in the Host Board connector. When MII is replaced by a new technology, all Host Boards deployed with MII would become obsolete. In addition, the ATC standards committee would have to reconvene to approve any new technology to replace the required MII.

ENGINE BOARD

Response to questions raised about Engine Board pin assignments

The Engine Board design must accommodate anticipated changes in processor technologies without performance degradations. In particular, the design must accommodate technologies employing high speed signals without at the same time introducing excess noise from spurious ground loops. Towards this end, two specific design changes were proposed by Clyde Neel of Naztec:

- Distribute power and ground pins on the interface connectors so that they are evenly spaced across the length of both connectors in order to provide a return current path near each signal (suggested pinout below), or
- Specify all signals at the interface to only be logic signals (e.g. HCT) with TTL thresholds, 5 volt tolerant, low DC current, and low capacitance. Do not specify any high-current, open drain signals. This implies that the final buffer of any non-logic level signals (e.g. LED driver, EIA485, etc.) is achieved on the Host board, not on the engine board. The benefits are two-fold: 1) it is better for high-speed logic, and 2) it increases the flexibility of the Engine Board by allowing the Host board to determine the final electrical form of signals leaving the host board, such as communication and user-interface signals.

Discussion

The Engine Board is proposed for this standard because it provides a cost-effective migration path for capability expansion and simplifies future changes to the core processing requirements of the ATC. In addition, the Engine Board design must be flexible enough to allow for customization of an ATC as needed by users. As such, the Engine Board can be expected to accommodate a variety of faster, more powerful processors, memory and serial channels over time. These components typically achieve their increased power and density through higher-speed elements.

Accommodating high-speed logic requires minimizing electromagnetic interference (EMI) and maximizing electromagnetic compatibility (EMC). The techniques for doing this are well documented in industry literature (see attached reference list). One design goal is to minimize the loop area formed by the path of current in a signal and its return path via the signal common. One way of accomplishing this is to distribute the power and ground pins so that no signal has to travel far to find a ground return.

Another technique for minimizing EMI would be to reduce the currents that flow or are switched on the board. This is the motivation for having only logic signals on the interface. It separates the functions of the Engine Board and Host by logical content. For example, if all the driver devices for SP1 through SP8 were on the Host board, then the Engine Board interface signals for the serial ports would all be logic signals. If the

same were true for the LED indicator signals, POWERUP, POWERDOWN, and LINESYNC, the Host Board would provide virtually all interface and driver functionality instead of the Engine board. Any interface could be altered on the Host Board, depending upon the application, without affecting the Engine Board.

In contrast to these concerns, we also received the following comment from George Chen, LADOT on 4-22-03: “In my opinion, the re-assigning all the pinouts for the engine board is not needed. I understand the argument for re-assigning the pinouts. However, if we look at the signal characteristics of the pins for the engine board, most of the signals are low speed signal as compared to CPU clock speed of 66Mhz to 2.4GHz (with the exception of 100BaseT Ethernet only if we required). We are not routing those clock signals straight out of the board. As far as the grounding and power pins, I think that a multi-layer board is required for any engine board design, and there will be individual ground and power planes in those boards.”

Conclusions and Recommendations

After careful engineering review, the consultant team concurs with the comments of George Chen of LADOT. The Engine Board pin configuration will remain as shown in the draft. However, the team agrees with Clyde Neel of Naztec that future problems will be mitigated in advance if we restrict the interface signals to 74HCT logic signals. Specifically on the Engine Board:

1. The CPU_RESET and CPU_ACTIVE open-collector outputs are changed to logic level, but retain their active-low polarity.
2. The Ethernet open-collector LED drive outputs are changed to RESERVED. The Ethernet indicator drive is now a function of the appropriate hub IC.

Details:

- The consultant team concludes that “... future technologies that incorporate high-speed logic...” have no effect on “...a return current path near each signal...” “
Specifically, increasing the processor speed does not affect the serial signals:
 - None of the four Naztec reference documents contain evidence to support the Naztec claim that processor speed somehow affects the Engine Board pins.
 - Although none of the Naztec documents contain a specific mathematical analysis of signal return current, our analyses show the Engine Board signal return current is mathematically independent of processor speed.
 - The LADOT comment is correct: 1) Engine Board signal speeds do not change when the processor speed increases from 66 MHz to 2.4 GHz. 2)

Every Engine Board high-speed signal already has a signal return (Ethernet, USB).

- The validity of the LADOT comment can be witnessed on every PC and PDA: Processors speeds have increased 1000-fold, while the COM1 serial speeds and pin assignment have remained the same. The Ethernet and USB signal speeds have increased by a factor of 10 without changing the pin configuration or adding multiple grounds, because each Ethernet and USB signal already has a return. The Draft Engine Board specification in this standard follows this precedence. We note that USB and Ethernet signals are balanced and differential and therefore provide their own signal return path.
- The consultant team further concludes that if we “...specify all the signals of the interface to be logic signals (e.g. HCT)...”, the frequency-domain signal return current of a higher-speed Engine Board actually decreases, specifically:
 - The rise time specified by the Motorola 68360 data sheet is much faster than the rise time specified by the Fairchild 74HCT data sheet.
 - The 2070ATC Engine Board transmits 5V 68360 signals, while the 3.3V signals of faster processors will be shifted to 5V using 74HCT logic. Therefore, the Engine Board with the faster processor will transmit slower rise and fall times, meaning lower frequency-domain signal return current.

Reconsider Engine Board connectors

Meeting attendees requested reconsideration of the connection of the Engine Board to the remainder of the ATC, with special interest in the use of a single 128-pin DIN connector. If the two connector design is retained, meeting participants requested an alternate means of keying the two connectors that avoids the use of keying pins. After careful consideration, the consultant team decided to **retain the Engine Board connectors as previously described**.

Discussion/Explanation

There was considerable discussion at the Houston meeting regarding the choice of Engine Board connectors. Concerns expressed included pin mechanical damage, electrostatic discharge (ESD) considerations, board keying, and mechanical integrity during installation and removal.

The interchangeable Engine Board is a key element of the proposed standard. As such, the Engine Board is similar to an EPROM memory device, which has no specialized connectors or keying techniques. Both must be handled with care during insertion and extraction, and in most cases will require special handling to prevent ESD damage. The

Engine Board is not an easily-removed rack-mounted assembly, nor is it intended to be inserted and removed with any regularity. It will likely only be exchanged as part of a structured upgrade program performed in a suitably-equipped signal shop.

Retaining the existing connectors allows distribution of the port connections to both sides of the board and provides inherent mechanical stability. Moving all electrical connections to one end of the Engine Board, particularly if considering the use of a four-row 128-pin DIN connector, will likely require the use of additional signal routing layers, smaller traces and smaller vias. These will likely make the Engine Board more difficult and expensive to manufacture and perhaps less reliable in its intended industrial application. In similar fashion, the Host Module may also require additional signal layers to accommodate the signal density of such a mating connector.

Reconsider Engine Board size to allow use on a 3U card

The consultant team examined the physical size of the Engine Board as it relates to its use in a 3U rack, such as is done with VME, and decided to **retain the size previously specified**. The Engine Board, as presently specified, will fit onto a standard 3U-sized card and that the resulting pair will slide into a standard set of 3U card guides. It might be necessary, depending on the card guides selected and the exact physical configuration, to remove the card guides in the adjacent rack slot to provide sufficient clearance. This was deemed an acceptable requirement.

Reexamine the Engine Board mounting height and overall envelope restrictions

The consultant team examined and discussed all of the physical characteristics related to the sizing of the Engine Board, its mating connectors, its relationship to the Host Module and the requirement that it provide backward-compatibility to the ATC-2070 A5 slot. The team also considered concerns voiced at the meeting in Houston regarding component height and placement. In response, the consultant team **modified the allowed component dimensions and placements. These are detailed in section 4.2.1 and on Figure 4-2 of Revision 2 of the draft standard.**

Other Engine Board issues

- Interface programming and test port pins

Manufacturers requested flexibility to designate interface programming and test port pins via proprietary on-board connectors

Resolution

- 1. The PROG_TEST pins designated in the interface specification will remain for use as previously described.**
- 2. Revision 2 allows the option of proprietary or design-specific programming and test connectors to Engine Boards as long as the Engine Board remains functionally interchangeable with Engine Boards designed by other manufacturers.**

- Standby power sources

Meeting attendees requested that standby power sources for real time clock (RTC) and SRAM be moved to the Engine Board and that required holdup time be specified.

Resolution

The considerable printed circuit board (PCB) 'real estate' required by the associated power storage components will unnecessarily burden Engine Board designs. Further, power storage and management is best handled by the controller's power supply. Therefore, **the standby power sources will remain as previously described.**

A careful examination of readily-available SRAM and RTC components indicates that the indicated holdup currents are reasonable and should provide sufficient additional capacity with anticipated SRAM decreases in memory densities and increases in memory sizes.

- Parallel interface

Although a medium-speed parallel interface was requested by certain meeting attendees for expansion purposes, the consultant team believes that **the serial interfaces already specified are better suited for anticipated future needs.** The consultant team investigated a number of possible parallel interface alternatives, most significantly the parallel interface typically found on a PC in its various manifestations, but found them not well-suited for general-purpose expandability due to insufficient addressability.

- Start-up time

The startup time specification is rewritten in Revision 2, in response to user requests, as the time from external application of controller power until the time the traffic application receives control of the unit hardware.

- POWERUP and POWERDOWN signals

The descriptions of POWERUP and POWERDOWN signals in Revision 2 now give additional details about the operation and handling of these signals.

- SYCLK_DIV_4

This signal has been removed in Revision 2, in response to user requests.

- More general designation of memory characteristics (e.g. FLASH)

The memory descriptions in Revision 2 have been generalized to permit the use of future technologies as they become available. In addition, the definition of FLASH memory in the Glossary has been made more general.

OTHER

Response to questions raised about overall controller size

A request was made to increase the maximum allowable vertical height of the NEMA version of the ATC Controller to allow larger displays because the NEMA TS-2 specification allows more than 7 inches of height.

After careful consideration, the consultant team decided that **the overall ATC Controller height in the draft standard will remain at 7 inches, but we invite further comments by users.**

Discussion:

- Every 2070N user we polled stated the 2070N size is too large because available cabinet shelf space is being lost to video and other ITS functions.
- Existing NEMA controllers with large displays already fit in a 7” vertical height.
- Instead of selecting an arbitrarily smaller size, we selected an ATC shelf-mount size that conforms to all of the following existing specifications:
 - NEMA TS-2, Shelf Mount
 - NEMA TS-2, Rack Mount
 - 2070ATC, Rack Mount for 332 Cabinets (2070-2A Field I/O)
 - 2070ATC, Rack Mount for ITS Cabinets (2070-2B Field I/O)
 - 2070ATC, Shelf Mount for TS-2 Type 1 NEMA Cabinets (2070-2N Field I/O)

In support of our design choice, we found the following design specifications for existing controllers:

NEMA TS-2 Specification, Paragraph 3.2.1 Dimensions:

The CU shall be capable of being shelf mounted. The CU shall also be capable of being mounted in a 19-inch rack (EIA Standard RS-310-C, 1982). The height of the CU shall not exceed 30.48 cm (12 in.). The depth of the unit, including connectors, harnesses, and protrusions, shall not exceed 36.83 cm (14.5 in.). On rack-mounted units, the mounting flanges of the control unit shall be so placed that no protrusion shall exceed 27.94 cm (11 in.) to the rear and 8.89 cm (3.5 in.) to the front.

2070ATC Detail Dimensions:

17” W x 10.25” D x 7” H for Enclosure, plus 2” W for Rack Mount Flanges

Performance benchmarks clarified

There is a need to specify/characterize and measure performance required of the ATC Controller and to expand the performance testing to describe a suite of benchmarks for all relevant controller subsystems. Discussions focused on the best way to accomplish this given the anticipated variations microprocessor selection allowed within the draft standard.

Response:

The minimum processors performance will remain 200 MIPS (based upon the MIPS rating given by microprocessor vendors in their data sheets) using Dhrystone 2.1

Discussion:

Dhrystone is a short synthetic (does nothing useful) benchmark program intended to represent the integer performance of a particular microprocessor. Dhrystone MIPS are the number of iterations per second of the Dhrystone benchmark relative to a VAX 11/780. This Dhrystone MIPS rating is greatly affected by compiler optimizations, which are allowed but not specified or controlled by the draft ATC Controller standard. As a result, Dhrystone MIPS comparisons can be highly suspect unless exact details of a particular compilation are known. Once known, the compiler optimizations may require further adjustments for a fair comparison.

The consultant team recognizes that MIPS may not be an accurate benchmark for a controller, which has a great deal of input and output processing unrelated to integer mathematics, but we are unable to find a more generally useful substitute that allows for the flexibility in microprocessor choice that is assumed in this standard. While not perfect, the published microprocessor MIPS rating provides a benchmark that contains sufficient accuracy to specify a general level of ATC Controller performance without requiring a particular microprocessor brand or clock speed.

Support requirements:

- The microprocessor vendor shall provide compiler and test program information in sufficient detail that the claimed Dhrystone 2.1 test results can be replicated.
- The controller address space containing the executable application software shall be accessed with zero wait states.
- The controller address space containing bootcode, operating system and data memory shall be accessed with wait states totaling 100 nS or less.
- The controller address space containing Input and Output devices shall be accessed with wait states totaling 1 uS or less.
- The bus widths shall be identical or wider than that used for the claimed MIPS rating.

Response to questions raised about removable data memory

Based on extensive user input, there is a widely recognized need for a removable memory device within the ATC Controller to provide setup data associated with that controller. This setup data must be available for download to the device when needed, and presumes there will be times when that data is not accessible via a network connection. This removable memory device must be robust with respect to device obsolescence and remote use by a variety of kinds of users and operational needs. The device is required only to store setup data, not application software, boot code, or an operating system.

Upon careful consideration of available alternatives, **the consultant team decided to retain the Data Key presently contained on 2070 controllers**. The consultant team recognizes this is a proprietary technology, but was unable to find any other technology that met the three critical requirements listed below:

1. Resistance to obsolescence

It was abundantly clear, based on the expressed user requirements on this issue, that the most important requirement was that the removable memory device and holder never become obsolete. Users consistently ranked concern over possible obsolescence of the removable memory device as a greater issue than reliability or any other factor.

The Data Key holder specified in the draft ATC Controller standard has been available under the exact same part number for 25 years, which is the reason the Navy and Air Force use Data Keys to arm weapons. Several vendors have committed to manufacture Data Keys if the current Data Key vendor goes away. Every Data Key holder on every deployed 2070 ATC is identical. Switching from the use of Data Keys to another kind of memory device would preclude a wide number of users from readily and easily moving critical data from a broken controller to a replacement controller in the field.

The Data Key memory can be tested continuously over the years by the controller to which it is attached. If a Data Key failure is ever detected, the controller continues to run normally, while alerting the user to replace and reload the key.

2. Robust Use

The Data Key is the only removable memory device with an open contact designed to wipe clean while the key is turned. USB and camera card contacts will clog when contaminated. The Data Key contacts can be cleaned with compressed air, or sprayed with contact cleaner and wiped with lens tissue.

3. Data Storage

Users require a removable memory device to store controller specific data (which may vary by controller application). For example, in the case of Traffic Signal Control, the Data Key stores intersection setup data. When replacing a broken controller with a new one, a technician typically removes the Data Key from the broken controller and inserts it directly into a new controller that replaces the broken one. The Data Key contains only the setup code required for the particular controller function(s) and does NOT contain new software or boot code that may not work in the new controller.

If DataKey is used, provide ‘media present’ and ‘power control’ signals

The signal DKEY_PRESENT is added to the interface specification of the Engine Board to indicate the physical presence of a key in the DataKey receptacle. However, a signal to control power to the DataKey receptacle will not be required on the Engine Board, as the 'media present' signal from the receptacle can be used by circuitry on the Host Module to control the application of power to the receptacle.

Extensive changes to environmental and testing details

Section 8 of Revision 2 contains entirely new material that is intended to be consistent with the ATC Cabinet in which it is anticipated this Controller will be housed. We invite comments on this section by all reviewers.

Inclusion of Performance and Material Requirements

Section 9 of Revision 2 provides requirements on the performance and composition of component parts of an ATC Controller. We invite comments on this section by all reviewers.

Inclusion of Quality Control section

Section 10 of Revision 2 describes Quality Control measures for an ATC Controller. We invite comments on this new section by all reviewers. For example, are sections needed on interchangeability, packaging, delivery, documentation, assemblies, workmanship, soldering, PCB traces, material design, or fabrication?

Revisions to Glossary

In response to various user comments, the Glossary has been extensively edited. We invite comments on this section by all reviewers. For example, do we need to reinstate definitions for any of the following terms: agency, A or ampere, cabinet, component, contract(or), engineer, equal, ma or milliamp, MIL, module, PCB, PVC, VAC, VDC? Is power failure/restoration covered adequately elsewhere, or is text needed in the glossary? Is it appropriate to include VME in the glossary?