

Following are our comments of the User Comment Draft Standard for the ATC Type 2070 v2.03:	Notes regarding comment
<p>General: Document as a whole needs to be modified to reflect Caltrans TEES dated June 8th, 2004. This includes the “final” version with the same date that occurred after June 8th. Additionally, TEES Detail 9-7-2 and/or 9-7-3 were modified in July but not widely distributed.</p>	<p>ATC2070 UCD Specific.</p> <p>Note that some items were discussed in the latest QPL meetings and Errata 2 addresses some of them.</p>
<p>Pg. 10, Section 2.4: Remove last paragraph since there is no such module as a 2070-1C nor is there a standard for one. This document also has no further reference/mentioning of one either.</p>	<p>ATC2070 UCD Specific</p>
<p>Pg. 10, Section 2.6: Remove second sentence in its entirety (a front panel is REQUIRED on all 2070s; which one is chosen is the optional aspect).</p>	<p>ATC2070 UCD Specific</p>
<p>Pg. 10, Section 2.6: Remove the word “only” in the last sentence.</p>	<p>ATC2070 UCD Specific</p>
<p>Pg. 11, Section 2.7: Change “form Factor” to either “model” or “option” in the last sentence. (The AGENCY cannot require a different form factor, but they may require, for example, that all power supplies must be -4A models regardless of the configuration of the other modules).</p>	<p>ATC2070 UCD Specific</p>
<p>Pg. 13, Section 3.1.3.1: Remove double period (‘.’) at the end of the last sentence.</p>	<p>ATC2070 UCD Specific</p>
<p>Pg. 16, Section 3.2.3: Need to add an allowance for using Supercapacitors (they cannot meet the 150% requirement). Suitable text is contained in the ATC v5a draft.</p>	<p>Impacts TEES Section 1.3.3 (page 1-3-2) also. ... Caltrans to correct.</p>
<p>Pg. 25, Section 3.5.1.3.1: I think that you mean 2 ounces per square foot (the actual translation from TEES is 1.8 ounces per square foot).</p>	<p>ATC2070 UCD Specific</p>
<p>Pg. 25, Section 3.5.1.3.2: Change “Theclass” to “The class” at the beginning of the second sentence.</p>	<p>ATC2070 UCD Specific</p>
<p>Pg. 26, Section 3.5.4: Suggest that jumpers BE allowed to enable a manufacturer to configure units as required for various installations. For example, to allow the inclusion of a 220/120 powers supply to be created. If required, standards could be placed on how jumpers are created but it must be remembered that both logic and power signals may need to be “jumped”. For example, with the issues surrounding Equipment Ground raised, we have added a “jumper” to connect Equipment Ground to the chassis.</p>	<p>Caltrans has agreed in principal that it would allow manufacturers to use soldered jumpers for option selection/module configuration purposes provided that they are not intended to be altered by field personnel.</p> <p>(Note several manufacturers have them, and seek informal “approval” afterwards only)</p>

Section 3.7 (in its entirety): Aspects of testing that relate to components NOT defined in this standard should be removed (references to additional components required to complete the testing of a defined device can be included, but they should not be tested). For example, subsections 3.7.13 to 3.7.20 inclusively should be removed.	ATC2070 UCD Specific
Pg. 51, Section 4.1.9: Suggest that address in range 128-254 are available for manufacturer specific use (and not reserved) to allow application specific accesses of non-defined external devices on the serial buses.	Caltrans agreed to alter address list to be compatible with TS-2 address allotment. I.e. 128-254 to be available for manufacturer use.
Pg. 52, Section 4.2.2.4: 1) state that the only use of ISO+12VDC on the 2070-1B module is to create the +5VDC for C13S and its related signals. 2) Add a Note #7 to Detail 4-7-7 (TEES 9-7-7) stating that +5VDC is to be derived from +12VDC-ISO for C13S (similar to Note #5 on Detail 4-7-8 (TEES 9-7-8)). 3) Also, reduce to 250 mA of +12VDC-ISO. Caltrans to advise how much current C13S +5VDC is capable of and whether current overload protection is required (and rating if applicable).	Some of these comments were discussed and resolved in Errata 2 already.
Pg. 52, New subsection of 4.2.2: The functionality of the signals on C13S is not properly defined anywhere. Suggest replicating (revised) sections 4.3.6.1 (also change to SP8), 4.3.6.3, and 4.3.6.4 within 4.2.2. Please also make corrections regarding isolation.	
Pg. 53, Section 4.2.3.4: SRAM requirements are different than for TEES 2002 with Errata. Suggest that TEES be generally adopted which states that 512KB of SRAM be included and nothing about RAM drive R0 (in this section). Discussions with Caltrans has them agreeing to change the minimum SRAM to be 1 MB with a minimum of 512KB being available to the agency. Furthermore, the balance of SRAM is to be available for vendor use with no restrictions on the flash sector backup size (i.e. the 150 KB limit needs to be removed from section 4.2.7.2.8) similar to Errata 2.	Caltrans has agreed to change to minimum of 1 MB SRAM, with 150KB max for flash sector backup, and minimum of 512KB available for agency.
Pg. 54, Section 4.2.3.6: In the last sentence, change the words “be align to” back to “provide” to agree with TEES. Use of the word “align” alters the meaning of the section.	ATC2070 UCD Specific
Pg. 54, 4.2.3.7: Need to specify the (minimum) length of the CPU RESET pulse.	Caltrans to specify both minimum and maximum pulse lengths.
Pg. 54, Section 4.2.3.10: Remove double period (‘..’) at the end of the last sentence.	ATC2070 UCD Specific
Pg. 55, Section 4.2.6: In the first sentence of the second	ATC2070 UCD Specific

paragraph, change “megabyte” to “megabit”.	
Pg. 56, Section 4.2.6: In the table, change “megabytes” to “megabits” in three places (one for each Key Type 3, 4, and 5).	ATC2070 UCD Specific
Sections 4.2.7.2 through 4.2.7.7.3 inclusively: Not checked at all ... assume working group has verified all details carefully.	Discussed clock and update issues (e.g. resolution, updating ticks/time/date asynchronously within an application program, synchronizing to a whole second hardware clock, etc). Caltrans to review and advise.
Pg. 70, Section 4.2.7.3.2: This section needs to reflect Errata 2. Additionally, the time from AC being applied (power switch toggled) to SYSRESET is undefined. Assumption from QPL discussions is a maximum of 0.5 seconds and this should be documented. For example, 2070 power supplies typically take 100 to 200 ms to stabilize, and then must maintain ACFAIL/POWER DOWN low for an additional 225 +/- 25 ms. This generates a 400 ms (approximately) delay before the CPU can be released from reset. Additionally, 2070 modules are supposed to be interchangeable between manufacturers and therefore manufacturer specific optimizations are not practical.	Needs to agree with Errata 2.
Pg. 73, Sections 4.3.1 & 4.3.2: Both sections refer to a VDC Power Supply (+12VDC to +5VDC) and drawing 4-7-8 indicates that +5 VDC is to be made available at pin 12 on connector C12S, but no where are there requirements placed on this supply (e.g. how much current, regulation, etc.).	Caltrans to advise including protection type and current capacity. Also need to modify 4-7-8 to agree with Errata 2.
Pg. 73, Section 4.3.3: Please remove the requirement of using “socketed firmware” ... most manufacturers are going to flash memory for software updates, and there are messages available that could be used to reflash the Field I/O module from, for example, C50S.	Caltrans to consider flash requirement via 2070-1 module.
Pg. 74, Section 4.3.4.2: This section has several errors. The second paragraph (on inputs) should be deleted in its entirety (section 4.3.4.1 addresses inputs). The third paragraph appears to be a cross of NEMA and 170 I/O standards and should be changed so that a LOW is from 0 to 4 volts, and change the transition time references to “logic 1” and “logic 0” instead of specifying voltages. You might just want to put the TEES wording back in (TEES section 9.3.4.1).	ATC2070 UCD Specific
Pg. 74, Section 4.3.5.2: This section refers to “Output Port 5, bit 8” which is a carry-over from the 170 days. Suggest that this reference be changed to “O39” (Output 39) to be consistent with 2070 terminology and how an application actually controls/references it during communications with the FCU.	

<p>Pg. 74, Section 4.3.5.2: One needs to specify the maximum time allowed between NRESET transitioning HIGH FCU active) and the start of the state changes. For example, NY State specifies a maximum “start delay” of 0.750 seconds (point of timing is unknown). Additionally, NRESET may not be the correct reference signal. Suggest that a reference point for the start delay needs to be made and that this reference needs to be relevant to other cabinet devices (e.g. the transition of both POWERUP and POWERDN to HIGH) otherwise the start of the watchdog transitions may not be performed in sufficient time. Furthermore, suggest that the time and reference be 250 ms from SYSRESET going HIGH. Since NRESET is based on the CPU RESET signal, its actual start cannot be used as the reference. Also, suggest that CPU RESET not cause the muzzle watchdog to be re-enabled for up to 10 seconds. Lastly, wording should be changed to “... every 100 ms for 10 seconds or until the first SET OUTPUTS command is received”</p>	
<p>Pg. 75, Section 4.3.5.3: There can be much confusion surrounding the “watchdog” operations on the FCU. As such, suggest that this watchdog be referenced as “FCUWDG” or “FCU Watchdog” in all locations. This includes this section, the FI/O status byte, etc. One should also comment that the “prescribed timeout” is determined by the manufacturer and that the operation of the FCU Watchdog is the responsibility of the manufacturer and not the User application.</p>	<p>Caltrans agrees in principal to name change for clarification purposes. Caltrans also agreed that FCUWDG should be dependent on FCU manufacturer requirements, and not the User Application.</p>
<p>Pg. 75, Section 4.3.5.3: Section states that a watchdog circuit be provided and section 7.1.1 (glossary) has the following definition for WDT:</p> <p style="padding-left: 40px;">WDT - Watchdog Timer: A monitoring circuit, external to the device watched, which senses an Output Line from the device and reacts</p> <p>Our first question is does the definition of WDT apply to the “watchdog” referenced in section 4.3.5.3? Note that the specific abbreviation is not used.</p> <p>If WDT does apply to the watchdog referenced in section 4.3.5.3, then our second question is as follows: If a manufacturer uses a device such as a Motorola MC68302 microprocessor that consists of a CPU (device being watched) and separate, but integrated, modules that include a watchdog timer that fully satisfies the requirements of section 4.3.5.3 do they need to also use an external watchdog device (i.e. not physically in the same package)? We suggest that they do not, provided that once the “internal” watchdog is enabled it cannot be</p>	

disabled.	
Pg. 75, Section 4.3.5.7: Section states that a LOGIC switch shall be provided. Is the use of a header jumper acceptable instead of an actual switch?	
<p>Pg. 75, Section 4.3.5.7 states that a LOGIC switch shall be provided and section 7.1.1 (glossary pg 113) has the following definition for LOGIC:</p> <p style="padding-left: 40px;">LOGIC - Negative Logic Convention (Ground True) State</p> <p>Question: Does the SP3 enable switch have to use negative logic within the Field I/O Module? As its function is strictly internal to the field I/O module, we suggest not.</p>	
Pg. 75, Section 4.3.5.7: Section 3.2.11.2 defines a LOGIC SWITCH and section 3.2.11.1 defines a DIP SWITCH. Please clarify that both DIP switches and LOGIC switches can be used for the SP3 enable switch.	
Pg. 75, Section 4.3.5.7 defines the functionality of the SP3 enable circuitry. Please clarify that if SP3 is disabled at C12S whether the SP3TXD +/- and SP3TXC +/- signals need to be tri-stated or can be held at logic '1'. (only one should be allowable for consistency).	
<p>Pg. 75, Section 4.3.6.1: Where is the isolation? Section is unclear as to whether each port is individually isolated, or whether SP5 is isolated and then split into two multi-drop ports (manufacturers have done both interpretations). Suggest the wording of the first sentence be "System Serial Port 5 (SP5) EIA 485 signal Lines shall enter the I/O Module, be isolated and then split into two multi-drop ports." This change would enable all signals on C12S to be referenced to the same voltage/ground reference.</p> <p>Furthermore, the operation of SP5 and the interaction with both the backplane, FCU and C12S needs to be explicitly defined. This includes the following cases:</p> <ol style="list-style-type: none"> 1) CPU transmits, state that both FCU and C12S are to receive the signals, 2) FCU transmits, state that both the CPU and C12S are to receive the signals, 3) C12S transmits, state that both CPU and FCU are to receive the signals, and 4) No one transmits, state that Field I/O must tri-state its transmit data and transmit clock (i.e. backplane SP5RXD and SP5RXC signals). <p>These cases need to be clearly specified so that SP5 appears as a true multi-drop port and so that SP5 is also useable by other devices in the other slots (e.g. A2).</p>	

<p>Lastly, operation when a 2070-2B is used needs to be defined so that SP5 is also available in slot A4 in a multi-drop mode when the -2B is in slot A3.</p>	
<p>Pg. 76, Section 4.3.6.2: The operation of SP3 as a multi-drop needs more clarity. Please specify the following cases:</p> <ol style="list-style-type: none"> 1) CPU transmits, state that C12S is to receive the signals, 2) Another device on the backplane (e.g. in slot A2) transmits, state that both the CPU and C12S are to receive the signals, 3) C12S transmits, state that both CPU and other backplane devices are to receive the signals, and 4) No one transmits, state that Field I/O must tri-state its transmit data and transmit clock (i.e. backplane SP5RXD and SP5RXC signals). <p>These cases need to be clearly specified so that SP5 appears as a true multi-drop port and so that SP5 is also useable by other devices in the other slots (e.g. A2).</p> <p>I am aware that a “SP3 Enable” switch is included per 4.3.5.7, but we should allow for true multi-drop if the user desires.</p> <p>Lastly, operation when a 2070-2B is used needs to be defined so that SP3 is also available in slot A4 in a multi-drop mode when the -2B is in slot A3.</p>	
<p>Pg. 76, Section 4.3.6.3: Where is the isolation? Section is unclear as to whether each signal is split first and then isolated (twice), or each signal is isolated and then split (manufacturers have done both interpretations).</p> <p>Suggest changing text to be “LINESYNC and POWER DOWN Lines shall be isolated and then split, one routed to FCU for shut down functions and the other changed to EIA 485; then routed to connector 12S for external module use.”</p>	
<p>Pg 76, Section 4.3.6.4: Please change the wording to state that “NRESET is the isolated OR of CPU RESET and POWERUP (SYSRESET)” to enable design flexibility (per some existing implementations).</p>	
<p>Pg 76, Section 4.3.6.6: Please use the correct signal names for consistency purposes (e.g. use DCG#1 instead of Ground #1).</p>	<p>ATC2070 UCD Specific</p>
<p>Pg. 76, Section 4.3.7: For clarity, please define what the “S” means at the msb position of byte 1 in the Input Transition Entry table. This could be also accomplished by defining “S” in section 4.3.8.1.</p>	

Note: “S” means the state of the input after the transition.	
Pg. 77, Section 4.3.8.1: What do bit 0, LSB and MSB refer to in the first sentence? The accurate references are to I0 to I63. Suggest that first sentence be changed to reflect this.	Caltrans agrees in principal to remove “bit 0”, “lsb”, and “msb” from the text. Therefore, change first sentence to “Input scanning shall begin at I0 and proceed to the next highest input.”
Pg. 77, Section 4.3.8.1: A comment about the filtering of inputs in section 4.3.8.2 should be added. Without the reference/note, section 4.3.8.1 requires that ALL (unfiltered) transitions be individually entered in the Transition Buffer.	Caltrans agrees that transitions must meet the filtering requirements for entry into the buffer.
Pg. 77, Section 4.3.8.2: Suggest that the end of the second sentence be changed to “ ... as noted above.”	Caltrans agrees in principal to comment.
Pg. 77, Section 4.3.8.2: Suggest that the table be modified to reflect the descriptive paragraph above it. For example, “Transition monitoring” should be changed to “Ignore input Flag” and “Filtering” should be removed (there is no such parameter ... the On and Off filter values control this).	Caltrans agrees in principal to comment.
Pg. 78, Section 4.3.8.3: Ref: line #3 (from top of page): When does the 2.0 seconds begin? Is it from the end of the last valid message from the CPU module, or is it from the end of the last response back to the CPU module?	Caltrans to review and advise ... Note: impacts both Field I/O module and CPU module (application programs).
Pg. 78, Section 4.3.8.4: In 2 nd sentence, change “milliseconds” to “millisecond”.	ATC2070 UCD Specific
Pg. 78, Section 4.3.8.4: At the beginning of the 3 rd sentence, change “An” to “A”.	ATC2070 UCD Specific
Pg. 78, Section 4.3.8.4: In 5 th sentence, change “>/=60” to “>=60”.	ATC2070 UCD Specific
Pg. 78, Section 4.3.8.4: In 7 th sentence, change “>/=500” to “>=500”.	ATC2070 UCD Specific
Pg. 80, Section 4.3.9.1.1: In Frame Types table, under 54/182, change “10.25 microseconds” to “10.25 milliseconds” in maximum message time column. Please verify ALL times under all cases.	
Pg. 80, Section 4.3.9.1.1: Complete the table by including all message/response codes. For example, instead of just stating what the manufacturer diagnostic frames are in the body of the text, please add them to the table. Also one should state the reserved codes (e.g. 44/172 to 48-176).	Caltrans agrees in principal to flesh out table for all possible entries.

Pg. 81, Section 4.3.9.2.1: For clarity, please change the description of “W” to refer to the “FCU Watchdog” or “FCUWDG”. (See comment regarding Pg. 87, Section 4.3.9.11).	Caltrans agrees in principal to suggested change. Caltrans also agreed to fix the order of the table so that it matches the bit order (bit order to remain unchanged for software compatibility reasons).
Pg. 82, Section 4.3.9.3: One needs to indicate what a ‘1’ means in the S bit. Append the following to the end of the 2 nd sentence “or ‘1’ on error”.	ATC2070 UCD Specific
TEES Section 9.3.9.5, page 9-3-10: Number of bytes (8 or 15) does not agree with table. Also in TEES 9.3.9.6.	Caltrans to address (e.g. split table).
Pg. 84, Section 4.3.9.5: Change title of 2 nd table (from top of page) to “Poll Raw Input Data Response (2070-2B)” to agree with text.	ATC2070 UCD Specific
Pg. 84, Section 4.3.9.6: In 4 th table (Poll Filter Input Data Response), change Type Number to 181 (from 180). Also, change binary representation appropriately.	ATC2070 UCD Specific
Pg. 84, Section 4.3.9.6: Change title of 5 th table (bottom of page) to “Poll Filter Input Data Response (2070-2B)” to agree with text.	ATC2070 UCD Specific
Pg. 85, Section 4.3.9.7: (Poll Input Transition Buffer Response table) Suggest that the “Byte Number” entry for the last five lines (Status ... MC Timestamp LSB) should be changed to “Byte 3(n-1)+...” where ‘n’ = Number of Entries. As currently written, the Status and full MC Timestamp entries are incorrect.	Caltrans agrees in principal to suggested change.
Pg. 85, Section 4.3.9.7.1: Change description of ‘C’ bit to “Indicates that transition buffer contained more than 255 untransmitted entries” or something similar. Current text sounds like an error occurred (it hasn’t ... one just needs to poll again for the balance of the transition entries).	Caltrans agrees in principal to suggested change.
Pg. 86, Section 4.3.9.7.2: Need to specify what happens on the very first poll since FCU power-up/reset. I.e. Should the FCU set the ‘G’ bit since the Block Number was not in sequence? What about if the CPU requests Block Number zero (0), in which case it appear to be re-requesting the same block (i.e. should we set the ‘E’ bit in this case)? Suggest that on reset (power-up), the FCU sets last block used to 255 and CPU begins by using block 0. This will provide monotonic sequencing immediately following CPU RESET/NRESET.	Caltrans to review & advise. Also how does E bit in 9.3.9.2 react during (power-on) reset?
Pg. 86, (new) Section 4.3.9.7.4: Need to add a new subsection to describe how a MC rollover entry is handled (i.e. set Input Number = 127).	Caltrans agrees (also add a new section to describe Timestamp per ATC2070 standard).

<p>Pg. 86, Section 4.3.9.8: Please clarify what is meant by “The output bytes depend on field I/O module”. This comment would make sense if there were different numbers of outputs being sent dependent on the type of FI/O, but this does not appear to be the case (as specified). Current implementations (and agency test programs) DO send different numbers of bytes (2070-2A = 8, and 2070-8 = 13). Suggest that you duplicate the tables, once for each FI/O type.</p>	<p>Caltrans agrees to separate tables for each I/O module type.</p>
<p>Pg. 87, Section 4.3.9.11: (Watchdog) What is the purpose of the “Configure Watchdog” command/response and how should it be used? For example, why is a User application running on the 68360 CPU module configuring the FCU hardware watchdog? The FCU hardware watchdog should be set and controlled by the FCU as it requires it for monitoring its own operation. Output 39 (O39) is the application watchdog in a 170 cabinet configuration and should be controlled by application as required.</p>	<p>Caltrans agrees in principal (previously discussed)</p>
<p>Pg. 87, Section 4.3.9.11.1: Who or how is the watchdog being “refreshed”?</p>	<p>Caltrans agrees (previously discussed that FCU watchdog is the responsibility of the FCU manufacturer ... User application should not be “refreshing” it).</p>
<p>Pg. 87, Section 4.3.9.12: Change the 2nd sentence to “Upon command, a response frame containing the 128 bytes of the Datakey is returned”. (also, make sure the period is included.</p>	<p>Caltrans agrees in principal to suggested change.</p>
<p>Pg. 88, Section 4.3.9.13: In 2nd sentence, change ‘... “3” is reserved for NEMA TS 2 Type 1 FI/O’ to ‘... “3” is reserved for 2070-2N (NEMA TS 2 Type 1 FI/O)’.</p>	<p>ATC2070 UCD Specific</p>
<p>Pg. 88, Section 4.4.1: In the 2nd sentence, change “external serial port connector(s)” to “external serial port connector C50S”. In the same sentence, also change “active” to “ACTIVE” for consistency throughout the text.</p>	<p>Caltrans agrees in principal to suggested change.</p>
<p>Pg. 88, Section 4.4.1: Option 3C refers to a connector “C60S’ whereas Detail 4-7-10 refers to C60P. Please correct as appropriate. Note, Caltrans has declared in Errata 2 that C60P is the proper configuration (i.e. it needs to be different that C50S).</p>	
<p>Pg. 91, Section 4.4.5.5: In 2nd line (from top of page), change “Page 9-7-12” to “Page 4-7-12”.</p>	<p>ATC2070 UCD Specific</p>
<p>Pg. 93, Section 4.4.5.16: For clarity, suggest using TEES text (9.4.5.16) and appending “(SP4)” to the end. Otherwise, one needs to clarify which connector pins 1 & 5 are on, and also remove the “s” from the word ‘Connectors’.</p>	

Pg. 93, Section 4.4.6: How long is one supposed to sound the bell upon receipt of a 0x07 (please state both minimum and maximum times)?	Errata 2 provides guidance
<p>Pg. 96, Section 4.6.2: There is an Equipment Ground connection from the power supply (PS2 pin 10) to the Serial Backplane. Should there be a trace on the backplane from this connection point to a screw hole, etc that connects to the chassis? It is also suggested that the Equipment Ground signal be routed to a pin on the backplane connectors for use by the modules installed in the A1-A5 slots, and also to the Front Panel connector. As an alternative to changing the front panel connector pin-out, we could add the requirement of a ground jumper wire from the main chassis to the front panel metalwork and/or PCB. In general, the whole issue of Equipment Ground needs to be addressed. Standard UL safety guidelines should be followed even if UL certification is not required. Also affects detail 4-7-5.</p> <p>Note: UL does not allow passing equipment ground through thumbscrews. Note: Caltrans recognizes UL at other places within TEES and one could therefore put the onus on Caltrans have their specifications meet UL requirements from a safety point of view (manufacturers are forced to make what Caltrans specifies).</p>	
Pg. 97, Section 4.6.4: This subsection excludes the use of the 5-slot VME cage ... please modify it to allow the use of the cage and 5-slot VME backplane (it only allows a one slot backplane). Need to fix wording to correctly allow 5-slot VME backplane.	
Pg. 98, Section 4.7: Change “Section Notes:” to read “All dimensions are in inches.”	ATC2070 UCD Specific
Detail 4-7-10: Note 4 must be changed to specify an example connector (e.g. xxx or similar equal) or type for the FP harness pin header in order to ensure the interchangeability (e.g. keying) that major customers are requesting. Currently, a manufacturer can choose any pin spacing, keying, etc they desire. Additionally, the location (front or back of each front panel and serial backplane needs to be specified (See Errata 2 for guidance)	
Detail 4-7-5: Fix spelling error in Note #7 (“enables”).	Caltrans agreed in principal to fix.
Detail 4-7-8: Where does the “signal” for C12S Pin 25 (EQUIP GND) come from/connect to? For example, on a 2070-2A there is no EQUIP GND signal on the serial backplane or either connector C1S or C11S. Also affects C13S on 4-7-7.	

<p>Detail 4-7-9: Remove the “port” columns/designations of all pins. These have no meanings since all I/O is referenced as “Ox” or “Iy” now. This comment affects both tables.</p>	
<p>Detail 4-7-10: What does the function of pin 1 of C60P mean? (“TO POWER B BOX”). In Errata 2, Caltrans has defined how much current at +5VDC-ISO pin 1 needs to provide. DC GND #1 to be changed to DC GND ISO, and SP6 RX/TX to be isolated also. Lastly, similar changes to C50S.</p>	
<p>Detail 4-7-10: Please change (correct) C50 connector type (Note #6) from “DB-9” to “DE-9”.</p>	
<p>Detail 4-7-10: What type of connector is used for C60P? (it is not defined anywhere). Suggest DE-9P. Checking the Caltrans “Introduction to 2070 Controller Hardware” (Materials Engineering and Testing Services), in Section III, item G, figure 28 shows C60 as “C60P” (on the Eagle example), yet the accompanying text and Figure 30 specify a “C60S”. Errata 2 now specifies connector as C60P (i.e. DE-9P).</p>	
<p>Pg. 99, Section 5: (Item #1) When one uses C50 Enable to disable channel 2, in addition to disabling the RS-485 signals TO the serial motherboard, does one have to also disable the RS-485 signals FROM the serial motherboard? I.e. can we leave SP4-TXD enabled and transmitting through the EIA-232 connector? Furthermore, ATC v5a section 6.3.2.1 states “... without ability to disable the transmitter” and that section is supposed to “represent the 2070-7A”. Note: Numerous suppliers of QPL’d products (e.g. 2070-6A) do not currently disable the output EIA-232 control signals (e.g. TX, RTS) but do disable the inputs (at the RS-485 circuitry). In Errata 2, Caltrans says to disable RS-485 both TO and FROM motherboard.</p>	
<p>Pg. 99, Section 5: (Item #1) Suggest that “C50 ENABLE” (Serial backplane A1:B21) should also be available on pin B22 of connectors A1 to A4 in order to allow SP4 to be disabled as necessary in the other slots (to support future ATC compatible modem modules).</p>	
<p>Pg. 99, Section 5: (Item #2) Do the EIA-232 drivers/receivers need to be in sockets if through-hole technologies are used? Or, is item #2 only applicable to the RS-485 drivers TO the serial motherboard? What about the RS-485 line drivers to the outside (e.g. on a 2070-7B or 2070-2B module)? Why do line receivers need to be disabled (if from the serial backplane) (4.2.4)?</p>	<p>Caltrans has stated in principal that EIA-232 does not need to be socketed.</p> <p>Caltrans has stated in principal that it wants both ends of RS-485 socketed.</p> <p>4.2.4: Caltrans to decide.</p>
<p>Pg. 99, Section 5: (Item #3) How fast must each EIA-232 circuitry reliably pass data through on the 2070-7A and</p>	

<p>2070-6x modules? We understand that the opto-isolation circuitry (and RS-485 interface to the serial motherboard) must work at speeds up to 1 Mbps (section 4.1.6), but what about the RS-232 signals? Please specify the minimum acceptable maximum data rates for the EIA-232 circuitry. Also, for clarity please change the 2nd sentence to start “Each module’s isolation circuitry shall ...”.</p>	
<p>Pg. 99, Section 5: (Item #4) Please clarify what “damage to operation means”. For example, can a communications module cause an operational communication “glitch” during hot-swap insertion/extraction that the system overcomes (e.g. retries)? In this case, no impact to final operation results ... just a harmless retry.</p>	
<p>Pg. 101, Section 5.1.4: Remove this subsection in its entirety as it is not part of Caltrans TEES and only works to restrict design solutions without adding major benefit. Yes, some manufacturers use a switch to turn on/off module power, but this is only their approach at trying to satisfy the requirement of Section 5, Item #4 (“The Comm modules shall be “Hot” swappable ...”). The use of a switch alone does not provide a soft-start feature and cannot guarantee meeting the Hot-swap requirement. Alternative, superior designs are better than a switch alone (e.g. hot-swap controller, soft-start power switches, etc)</p>	
<p>Pg. 101, Section 5.2.2: Please change (correct) connector type (last sentence) from “DB-9S” to “DE-9S”.</p>	
<p>Pg. 101, Section 5.2.3: Please change (correct) connector type (last sentence) from “DB-15S” to “DA-15S”.</p>	
<p>Pg. 101, Section 5.2.3: Spelling error – In third line, please change “drive/receiver” to “drive/receive”.</p>	
<p>Pg. 102, section 5.5: Change section “notes” so state dimensions are in inches and also convert tolerance to inches. Alternatively, one could remove all section notes since they are irrelevant (i.e. there are no dimensions within the section).</p>	
<p>Detail 5-5-1: Change (correct) note #1 to reference Detail 4-7-6.</p>	
<p>Detail 5-5-1: Change EIA-232 signal names in connector pinout table to agree with section text. I.e. Change “CD” to “DCD”. Also change “DATA IN” and “DATA OUT” appropriately.</p>	
<p>Detail 5-5-2: Change (correct) note #1 to reference Detail 4-7-6.</p>	

Detail 5-5-2: Change (correct) connector type for 2070-7A. In 2 places (table heading and in Note #2), change “DB-9S” to “DE-9S”.	
Detail 5-5-2: Change (correct) connector type for 2070-7B. In 2 places (table heading and in Note #2), change “DB-15S” to “DA-15S”.	
Pg. 103, Section 6.1.1: Change “specification” to “standard”.	
Pg. 103, Section 6.1.1: In 2 nd line, change “NEMA TS1” to “NEMA TS1/TS2 Type 2”	
Pg. 103, Section 6.1.2: Please fix brackets in Type 2070-5 line (this may already have been based on a verbal comment made earlier).	
Pg. 103, Section 6.1.3: Please fix brackets in Type 2070-5 line (this may already have been based on a verbal comment made earlier).	
Pg. 103, Section 6.2.1: Please convert “Byte 9 Bit 6” to the appropriate Ox. Currently it is unclear whether the standard refers to the 9 th byte within the message or the 9 th output byte. I believe that it should be 078 (please verify).	
Pg. 104, Section 6.2.3: Please correct (change) connector type from “DB 15S” to “DA 15S”. Also need to add requirement for latch blocks. For reference, here is the NEMA TS 2 relevant to that connector. ” The Port 1 connector shall be a 15 pin metal shell D sub-miniature type connector. The connector shall utilize female contacts with 15 millionths of an inch minimum gold plating in the mating area. The connector shall be equipped with latching blocks. The connector shall intermate with a 15 pin D type connector, Amp Incorporated part number 205206-1, or equivalent, which is equipped with spring latches, Amp Incorporated part number 745012-1, or equivalent.”	
Pg. 104, Section 6.2.4: Please add requirement that EQ GND also be routed to the faceplate.	
Pg. 104, Section 6.2.7: In Connector A table, please correct placement of Pin “J” and its function (“NA”). Currently, Pin F has Function “Fault Monitor J” which should be “Fault Monitor”.	
Pg. 105, Section 6.3.1: Please change the first sentence to start “The 2070-4N (A or B) ...”	
Pg. 105, Section 6.3.1: In the 2 nd sentence please correct the reference from “2070-4N (A and B)” to “2070-4 (A	

and B)”. 	
Pg. 106, Section 6.4.4.1: Change “Specification ...” to “Per Section ...”	
Pg. 106, Section 6.4.4.2: Change “Specification ...” to “Per Section ...”. Also change 2 nd “specification” to “section” and fix reference (TEES reference is wrong also).	
Pg. 106, Section 6.4.6: At beginning of sentence, change “A” to “All”.	
Pg. 107, Section 6.4.8.1: Need to add specification of Ground True, “1”, less than 8 volts (to agree with NEMA TS 2).	
Pg. 107, Section 6.4.8.1: The last sentence (concerning LINESYNC) should be moved to its own section (e.g. 6.4.8.3) to be consistent with section 4.3.	
Pg. 107, Section 6.4.8.2: From what EIA-485 port do the signal lines originate from that get routed to the EX1 connector (SP3 or SP5)?	
Pg. 107, Section 6.4.8.2: Change “17” to “18” to agree with number of pins used.	
Pg. 107, Section 6.4.8.2: Do the EIA-485 signal lines going to EX1 need to be isolated again? (they are already isolated once on the 2070-2B module). If SP3 is the port then suggest that no further isolation/circuitry is required (just pass them through). Alternatively if it is SP5 then suggest the following signal routing: From HAR 1, the EIA-485 signals are split with one path routed directly to EX1 and the second path isolated to feed the FCU. This approach requires the least number of components.	
Pg. 107, Section 6.4.9: Where does the EIA-232 Serial Port go to? What is its purpose? Is it somehow connected to SP3 or SP5? If it goes to SP3 (or SP5), then how do we use the baud rate selector jumpers?	
Pg. 107, Section 6.4.10: This section implies that a 2070-6x module must be supplied with a 2070xN(1 or 2) controller. Please insert the word “optional” before “Model 2070-6” in the 1 st sentence.	
Pg. 107, Section 6.4.11.1: Insert “Conceptually,” at the beginning of the first sentence.	
Pg. 108, Section 6.4.11.2: What is causing FCU Port 10, Bit 7 to change state every 100 ms? If it is the “User”	

<p>application then say so. If it is the FCU embedded firmware then say that (and require that the FCU be automatically reset). Regardless, change “FCU Port 10, Bit 7” to “output Ox”. Please clearly specify what “x” is. Calculations indicate it is either O78 or O79 (depending on whether bit numbering starts at bit 0 or bit 1) but these are already allocated (section 6.4.11.5) as FAULT and VOLTAGE respectively.</p>	
<p>Pg. 109, Section 6.4.11.6: For clarity, please reword Item #5 (“Performs items 2 & 3 above User software”).</p>	
<p>Pg. 109, Section 6.5: Suggest that a drawing of the 2070-2N module be included (it is the only module without a drawing).</p>	
<p>Pg. 109, Section 6.5: Change “Section Notes” at bottom of page to state that dimensions are in “inches” (not millimeters) and also convert the sheet metal tolerance to inches.</p>	
<p>Detail 6-5-1: Convert dimension in Note #4 to inches (2.286 mm = 0.09 inches).</p>	
<p>Detail 6-5-3: Change title of drawing from “ISO” to “ISOMETRIC”. (Note: Glossary defines “ISO” which is in consistent with its use here).</p>	
<p>Detail 6-5-4: Replace detail page with detail 11-5-4 from TEES (wrong detail drawing was used).</p>	
<p>Detail 6-5-4 (revised): Change the “PORT-BIT” column to reflect the Output or Input Number (e.g. Ox or Iy). This is how the User software will actually address (control/read) them. (There are no “ports” per se.)</p>	
<p>Detail 6-5-5: Change the “PORT-BIT” column to reflect the Output or Input Number (e.g. Ox or Iy). This is how the User software will actually address (control/read) them. (There are no “ports” per se.)</p>	
<p>Detail 6-5-6: On connector EX1, please clarify where the EIA-232 signals come from (pins 2, 3, 4, 5, and 8). I.e. which port, etc?</p>	
<p>Detail 6-5-6: On connector EX2, please clarify where the EIA-485 signals come from. I.e. which port (SP3 or SP5)?</p>	
<p>Detail 6-5-6: On connector EX2, where do the two “EQ GND” pins get their signal from (neither C2 or C20 of a 2070-6x module has EQ GND on them)?</p>	
<p>Detail 6-5-6: On connector EX2, where do the two “DC</p>	

GND #1” pins get their signal from (neither C2 or C20 of a 2070-6x module has DC GND #1 on them)? Should this be “ISO DC GND” (from the 2070-6x module)?	
Pg. 112, Glossary: Please check use of “I.D.” for consistency within document. In one location I saw “I D”, unsure of others.	
Pg. 112, Glossary: Please enhance “ISO” definition so that it tells the reader that we are not referring to the standards body.	
Pg. 112, Glossary: Please reword “jumper” definition for clarity. The first “conductive” is wrong. Consider replacing with either “conductor” or “conductive points”.	
Pg. 113, Glossary: Please check for consistent use of “LOGIC” throughout the document. For example, section 5.1.2 refers to “LOGIC” switches but they are not necessarily consistent with this definition.	
Pg. 113, Glossary: Request that the screw recesses of the Thumb Screw Device be changed from “Slotted” to “Phillips/Slot Combination”. This request will also assist in rationalizing the use of tools throughout the document. For example, both sections 4.6.1.2 (pg. 96) and 6.4.1 (pg. 105) require the use of Phillips flat head to screws. Several major agencies require compliance to the standard, yet they also require the ability to use a Phillips head screwdriver (conflicting requirements). Recommend changing part numbers to: TSD No. 1 – 8-32 SOUTHCO #47-62-381-20 or equal. TSD No. 2 – 8-32 SOUTHCO #47-62-381-80 or equal. TSD No. 3 – 8-32 SOUTHCO #47-82-181-10 or equal.	
On 2070-1B connector C13S Detail 4-7-x, +5VDC cannot be referenced to DC GND #2. Suggest deriving +5VDC from +12VDC-ISO similar to on 2070-2A	
On 2070-1B connector C13S Detail 4-7-x, there are NRESET +/- signals which are not described anywhere in section 4.2 and in particular section 4.2.2. Suggest adopting text from 4.3.6.3 as appropriate. Also, do these signals need to be isolated (recommended).	
On 2070-1B connector C13S Detail 4-7-x, there are LINESYNC +/- and POWERDN +/- signals which are not described anywhere in section 4.2 and in particular section 4.2.2. Suggest adopting text from 4.3.6.3 as appropriate. It is simple to generate a RS-485 signal from the TTL backplane signal, but these signals should be isolated also (recommended).	