ATC 3000 Standard

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Section 1

General

1.1 Scope

With the growth of intelligent transportation systems (ITS), transportation management increasingly relies on electronically controlled devices deployed in the field and the controllers that coordinate and relay data from those devices. The ATC-3000 provides communication, control, and data gathering from and to

- Central control computers when appropriate
- Other ATC-3000 controllers when appropriately configured
- Control units for devices deployed in the field, typically in the vicinity of and linked to the controller.

Essentially an ATC-3000 is a special function computer that must be able to operate remotely in a largely unattended mode in the harsh environment of field deployments throughout the United States.

The goal of this standard is to provide a next generation open architecture design for such a transportation controller. The ATC-3000 design is based on the concentration of computing power in a single component (the Engine Board) that, if compatible with this standard, is interchangeable with Engine Boards designed by other manufacturers. Second, the standard provides for required and optional features, all of which are based on open standard, common protocol communication standards. Third, the ATC-3000 standard is responsive to all functional requirements identified in Section 3 below. Finally, design specifications are given where needed to ensure plug-in compatibility between modular components of the ATC-3000.

Figure 1 provides details of the component parts of the ATC-3000 and their connections.

>>>>>> (PDF FILE ATC3000.pdf SUPPLIED SEPARATELY)

1.2 References

2.8.1 Normative References

This standard assumes and is consistent with known versions of ATC-3000 cabinet (GIVE REFERENCE WHEN AVAILABLE) and ATC-3000 API (GIVE REFERENCE WHEN AVAILABLE) standards.

1.2.1.1 ATC-3000 Controller Environmental Specification

1.2.1,2 ATC-3000 API Specification

1.2.1.3 USB Specifications

Universal Serial Bus Specification. Revision 1.1, September 23, 1998. Copyright © 1998, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, NEC Corporation. All Rights Reserved.

http://www.usb.org/developers/docs/usbspec.zip

USB Mass Storage Overview 1.1

http://www.usb.org/developers/devclass_docs/usbmassover_11.pdf

USB Mass Storage Bulk Only 1.0

http://www.usb.org/developers/devclass_docs/usbmassbulk_10.pdf

USB Mass Storage Control/Bulk/Interrupt (CBI) Specification 1.0

http://www.usb.org/developers/devclass_docs/usbmass-cbi10.pdf

USB Mass Storage UFI Command Specification 1.0

http://www.usb.org/developers/devclass_docs/usbmass-ufi10.pdf

1.2.1.4 Ethernet 802.3 Specifications

IEEE 802.3-2002 Specification

http://standards.ieee.org/getieee802/download/802.3-2002.pdf

2.8.2 NTCIP Standards

This standard adheres to all relevant NTCIP standards for communication protocols in ITS devices.

1.3.1 Contact Information

Upon acceptance of this standard, contact ITE (information to be supplied)

1.3 Glossary of Terms (TO BE ADDED LATER)

Section 2

ATC 3000 Concept of Operation

This section defines the user needs that the subsequent sections within this standard will address. The first step is to identify the problems being addressed by this standard. In this particular case, a general purpose field located computing device is the subject of the standard. The device must be capable of executing applications software from various developers whether they are consultants, agency employees or those of commercial product firms.

Generally accepted systems engineering process starts with an identification of the ways the system will be used. In this case, the applications functionality and associated needs of the devices meeting this standard depend on the particular applications software loaded into the device at deployment time. Therefore, the details of particular future applications use case are not completely known at this writing. It is important nonetheless that the support and usage needs of the most commonly known and anticipated applications be defined.

As indicated above, it is the intent of this standard to describe a general purpose computing device, and as such, the ATC 3000 CU can be thought of as somewhat analogous to a Personal Computer (PC). A difference from the PC is that a device meeting the ATC 3000 CU standard must be able to withstand the harsh environment of a field located control cabinet with no special cabinet or environmental conditioning. Another difference is that the ATC 3000 CU must be able to operate remotely in a largely unattended mode. Similar to the PC, the ATC 3000 CU must adhere to a set of programming conventions and interfaces standards such that the applications software that runs in the device can be developed independently of the hardware.

This is a standard not a sales pitch.2.1 Problem Statement

One of the largest component costs of today's Intelligent Transportation Systems is associated with the development, testing, deployment and maintenance of applications software. Additionally, as the current trend continues towards distributing more of the intelligence of ITS out closer to where the problems exist, in the field, there is an increasing demand for more and more capable field deployable devices. This hardware must run more sophisticated applications software and operate in modern networking environments. The ATC 3000 is intended to address these needs.

The ATC 3000 CU is intended as a, next generation, "Open Systems" controller which follows the "Open Systems" lineage of the current ATC 2070 CU and older California/ New York Model 170 controllers Think about this wording as it could be taken as "anti-

NEMA" We need to find some good political wording to serve both camps. "Open Systems" in this context refers to the concept of separation of hardware from software such that the interface between the two is standardized so that software can be developed independent of the hardware. "Open Systems" help protect an agency's investment by guarding against premature obsolesce due to a manufacturer's discontinuance of a particular line of equipment or the manufacturer's ceasing of business operations altogether. Additionally, with an "Open Systems" Please find a common **standard** definition for Open Systems that can be used as a reference. In the computer industry these two words are getting to the point where they are meaningless clichés. An internet search on "open systems" revels a just how over used these words are. Try this one: http://www.sei.cmu.edu/opensystems/faq.html <<<This is from Carnegie Mellon's Software Engineering Institute. where hardware interfaces are generically defined and standardized and adopted by multiple manufacturers, equipment procurement competition is typically increased; resulting in reduced procurement costs. Deployment, integration, and maintenance costs are also generally reduced because of the commonality and interchangeability of units between various manufacturers reducing spare inventories and technician training costs.

Another important need for "Open Systems" field controller units has to do with the occasional need for custom, specially built, applications. Sometimes the demand for a particular application or custom feature is too small, from an industry-wide standpoint, to be of much interest as a product for manufacturers. Nonetheless, a particular problem or research need may require some unique functionality. With "Open Systems", a user can write, or have someone else write their own software to satisfy a unique set of requirements. Furthermore this can be done this without special support or permissions from the hardware manufacturer.

2.2 Historical Background

The Model 170 CU

The Model 170 CU was developed in the mid 1970's to address needs discussed above for an "Open Systems" controller for transportation applications. The Model 170 obtains its hardware / software independence by requiring, by part number specification, the use of a couple of specific integrated circuit chips (for CPU and Serial Communications functions). In addition, a memory mapped I/O scheme was defined so software developers would know precisely where to address input and output functions regardless of who manufactured the hardware unit.

While the Model 170's architecture has been enormously successful and achieves the desired independence of the hardware and software, the Model 170 relied heavily on specified Motorola CPU and serial communications chips (or suitable substitutes). Unfortunately, these two chips and their associated family of chips have been designated for phased-out obsolescence. The issue is further compounded by the relatively poor computational performance of the Model 170, compared to today's controller systems. This has required applications software written for the Model 170 CU to be coded in assembly or machine language and makes it difficult to move software applications

written for the Model 170's architecture to more modern system architectures. Also, the Model 170, without an external CPU, can also not handle the performance demands of today's modern packet based high speed communications networks. Few options currently exist for agencies heavily invested in Model 170 software/hardware architecture to preserve their investments in Model 170 applications software going forward.

The 2070 ATC CU

The 2070 ATC is a current generation "Open Systems" controller system. It was originally developed by Caltrans and City of Los Angeles to address some of the shortfalls associated with the Model 170 as discussed above. Its designers tried to mitigate some of the potential parts obsolesce issues which plague the Model 170. Instead of relying on the efficiency of assembly language programming, the ATC 2070 CU includes the necessary resources to execute programs written in higher level programming languages such as ANSI C or C++ (BI Tran would claim that their software for the 2070 is written in C and it just happens to be complied to the 6802 assembly language. Soooo don't we already do this? Maybe one of the significant issues is the more powerful set of cpu commands for more advanced features in these new cpus.. Such higher level language programs are more easily ported to other hardware platforms should that be necessary. The ATC 2070 CU also specifies the use of a specific Operating System (OS-9) to separate the hardware from the application software. By specifying a particular OS, fixed memory mapping of User and Field Input/Output, as done with the Model 170, is no longer necessary. The OS and associated standardized support functions take care of many of the basic execution management and scheduling tasks required by application software programs. The OS further extends the hardware/software independence through I/O and memory resource sharing capabilities. These capabilities allow multiple independent applications to be run simultaneously on a single controller unit in a multi-tasking mode. This was not the case with a Model 170.

The ATC 2070 CU standard also provides for greater subcomponent interchangeability and modularity than the Model 170. Model 2070 component modules are defined through specification such that they are interchangeable among different manufacturers. These component modules are as follows:

With the Model 170 only the Modem/Communication module and the plug-in memory card are interchangeable among different manufacturers.

On the negative side, the ATC 2070 CU specification requires that only a specified CPU chip be used in its design. The ATC 2070 CU goes further and requires that a particular commercial Operating System be used. Unfortunately, the embedded hardware and Operating Systems market place is not as large and tied to a single vendor's concept as is the PC marketplace. As a result, longevity concerns are surfacing for the ATC 2070 related to the Operating System and CPU chip architecture selections chosen for the ATC 2070. Potential adopters are concerned that additional retrofit and software porting costs would be required should either the Operating System or the CPU utilized by the ATC 2070 be no longer available. The 2070 also dictates a very specific package and component arrangement.

2.3 Fundamental Needs

Addressing the longevity concerns surrounding the ATC 2070 CU is a principal need to be addressed by the ATC 3000 standard. In particular, with the today's accelerated pace of microprocessor technology advancements and quicker product obsolesce cycles, it is very desirable not to specify one particular CPU chip set or one particular OS environment, a single package/enclosure style as well! This thing has to fit legacy cabinets as well as any future ones and not just the ITS cabinet. It also has to accommodate future operator interfaces. as is done with the ATC 2070 standard. To achieve the greater level of CPU and OS independence from applications software an Applications Programming Interface (API) is required. An API is a set of standardized software functions which applications can use for the management, control and interfaces to hardware and standard OS functions.

A separate but coordinated standards effort is defining a standardized API for ATC use. The concept is a two layer approach as shown in Figure 1.1. At the lower level, functions are provided that encapsulate and hide the implementation details of a particular OS or hardware selection. At the higher level, a set of generic functions are available that make use of the lower level functions to perform higher level user interface and management functionalities. The API separates the application program from the hardware and Operating System in such a way, to break the tie to a single Operating System or CPU chip family for the controller. It is desirable for the ATC 3000 to incorporate by reference this API standard.

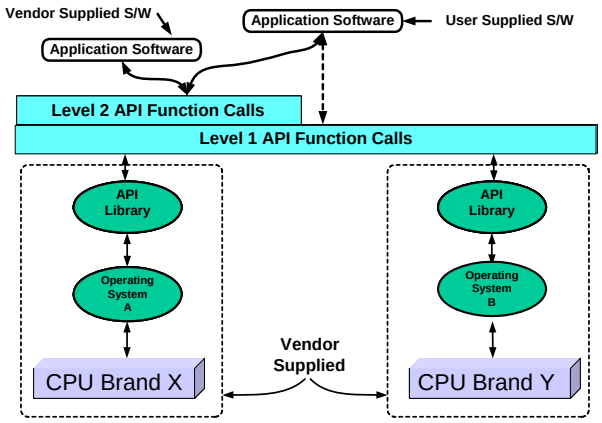


Figure 2.1 Two Layered API Architecture

An additional need for the ATC 3000 is improved network communication interface support. Advanced communication capabilities are becoming increasingly important for ITS field controllers. ITS data communications networks are deploying NTCIP and Internet Protocol (IP) based data communications networks. Peer to Peer networking capabilities are also increasingly required for advanced control algorithm

implementations. For such networks, Ethernet is the connection interface of choice at field controllers. Additionally, communication equipment connections are moving from the older 10Mbit/sec interface rates to a 100Mbit/sec standard. The current ATC 2070 ATC supports an integral 10 Mbit/sec interface but not the increasingly more common 100 Mbit/sec interface.

Improved affordability is also a goal, particularly for fixed and predefined ITS applications where subcomponent interchangeability is not as important and may be traded off for simplicity of design, smaller size, and/or reduced deployment costs. It is desirable for the ATC 3000 standard to provide enough flexibility in form factor and packaging as to allow manufacturers to offer complete families of designs all of which are application software capable and meet a minimum set of ATC 3000 design standards. As is the case with Personal Computers, many different hardware configurations and designs are envisioned all which would share basic applications software and external interface compatibilities.

Finally, a further need exists for controller units meeting the standard to be field upgradeable allowing agencies to cost effectively take advantage of future CPU, serial communications, driver, and memory chip improvements without necessitating the complete change out of other controller components. To this end, a standardized subcomponent interface is required that defines the form, fit, and function of a circuit board with CPU, serial communications, driver and memory components (referred hereafter as the Engine Board). For further protection against obsolescence, requirements should dictate needs to insure interchangeable of Engine Boards among various manufacturers' controller units.

2.4 Operation Environment

The traffic system operator interfaces to an ATC through one of three mechanisms:

- Central computer – this type of operation configures and manages ATC applications from a computer located at a traffic management location, such as a Traffic Management Center (TMC).
- Local computer – this type of operation performs the same functions as a central computer does, but uses a portable interface device (e.g., laptop, PDA, etc.) connected directly to a port of the ATC.
- Locally – this type of operation uses the front panel or portable interface devices (e.g., keyboard, displays, switches) at the ATC to perform the functions of configuring and managing the ATC applications.

The connection between the central computer and the ATC runs over a telecommunications network, which can be either wireline or wireless in nature. The network interface at the ATC can be either a serial communications port or Ethernet port. Figure 2-2 depicts the physical architecture of the key components related to a typical ATC based system controlled from a central location.

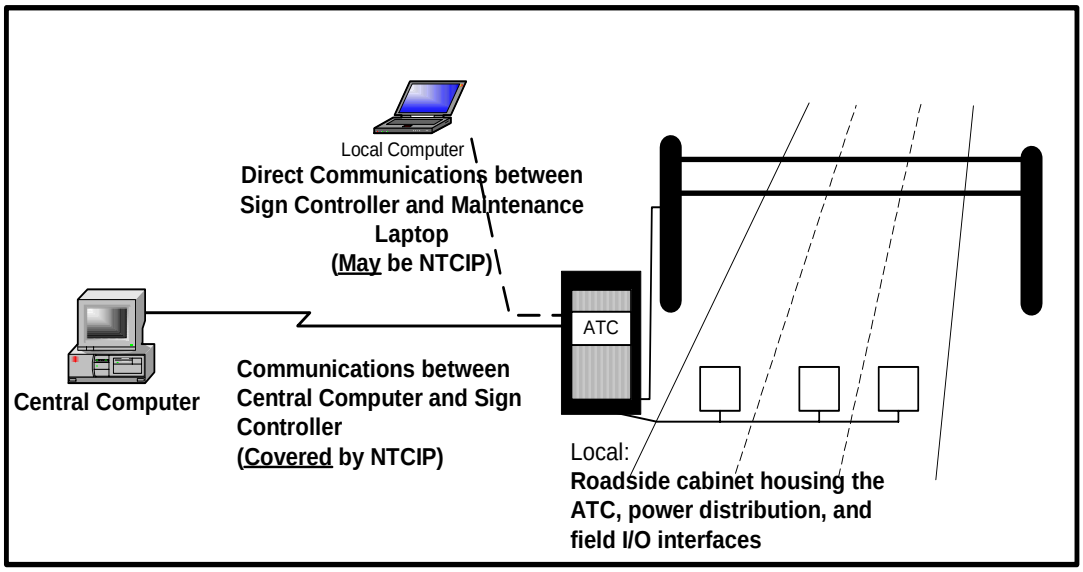


Figure 2-2: View of a Typical ATC System Environment

The ATC is enclosed in a field located cabinet. The ATC connects to other cabinet located input/output devices (i.e. load switch racks, detector racks, etc.) through serial and or parallel connections. Cabinet input/output devices, in turn, connect to field located elements (i.e. signal head, dynamic message sign, sensors, etc.).

In practice, there are additional components in a field cabinet which support the system including power distribution equipment, monitoring devices, and terminal facilities. The exact device interfaces and cabinet configuration depends on the particular ATC application and type of equipment being deployed.

As a minimum, the ATC 3000 CU must provide the necessary interfaces to support the new ITS Cabinet standard. Additionally, the ATC 3000 CU should provide optional interface support for common legacy cabinets including Model 170, NEMA TS1, and NEMA TS2 types.

2.5 Representative Usage

As previously indicated, the functionally of a deployed ATC 3000 CU will depend on the applications software loaded into it. Typical applications to be hosted on the ATC are listed in Table 2-1.

- Traffic Signal
- Traffic Surveillance
- Ramp Metering
- Data Communications
- Field Master
- Lane Use Signals
- Speed Monitoring Station
- Freeway Lane Control
- Incident Management Station

Table 2-1 ATC Applications

Due to the general purpose nature of ATC's, many future, but currently unanticipated, applications will likely be deployed with the ATC 3000 CU. As a result, the operational needs for every application are not fully known or completely identifiable at this time. Nonetheless, a number of basic operational usage scenarios can be gleamed from the most common and expected applications.

This section identifies and describes some of the most common "use cases" to be supported by the ATC 3000 CU and its associated applications software. Figure 2-3 provides a top-level view of the operational features offered by a typical ATC application. Figure 2-4 provides a top-level view of important maintenance and upgrade features. The definition of each feature is provided after the presentation of the diagram. The features in this diagram are subdivided into more detailed features in the text below. For these "use cases", a more detailed "use case" feature diagram is presented along with corresponding definitions. Section 3 then uses these definitions to organize and define the various functional requirements of an ATC CU.

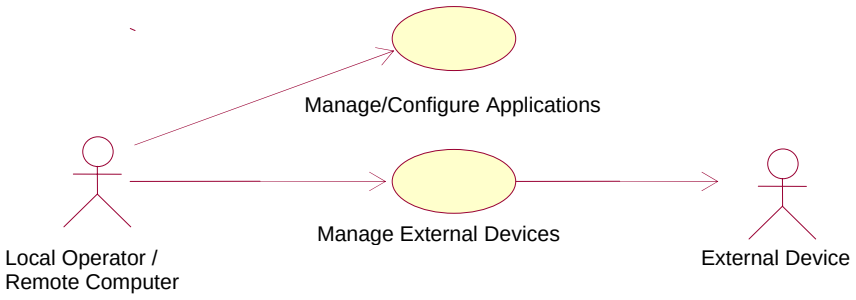


Figure 2-3: Main Operations Feature Diagram

The generalized operational features of an ATC can be categorized into two major areas:

- Manage/Configure Applications

- Manage External Devices

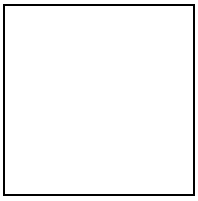
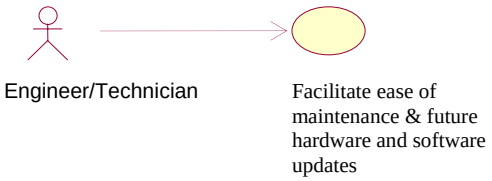


Figure 2-4: Main Maintenance/ Support Diagram



The Maintenance and Support function includes features for maintenance and update/enhancement of the controller unit's hardware and/or software.

Manage/Configure Controller Applications

The various sub-features for managing and configuring software applications are shown in the following figure. The subsequent sections detail these subfeatures

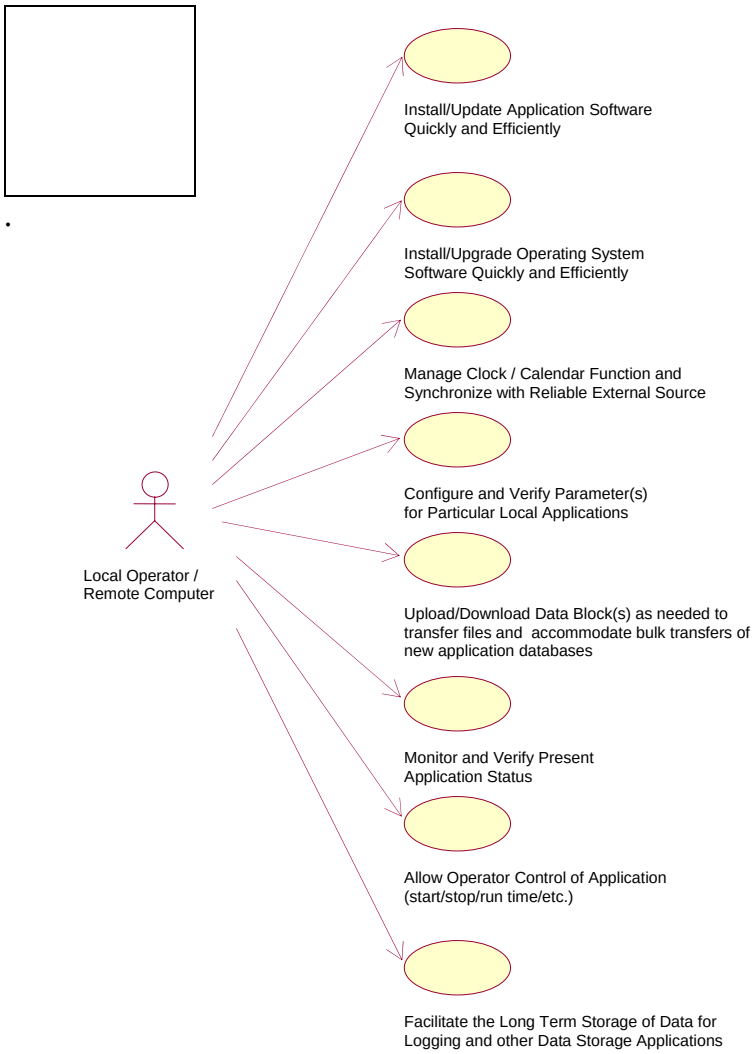


Figure 0-5: 'Manage/ Configure Applications' Subfeature Areas

Install/Update Applications Software Quickly and Efficiently

This feature allows the local operator or a remote computer to install or update the application software resident on the ATC.

Install/Upgrade Operating System Quickly and Efficiently

This feature allows the local operator to install or update the Operating System software resident on the ATC.

Manage Clock / Calendar Function and Synchronize with Reliable External Source

This feature is responsible for management of a real-time clock calendar function within the ATC. It allows the operator or a remote computer to interrogate and/or update the current time and date information kept by the ATC. It is responsible for synchronizing the ATC's Operating System's clock to the power line or other suitable locally available reference to adjust for internal ATC clock drift.

Configure and Verify Parameters for a Particular Local Applications

This feature allows the operator or a remote computer to manage and update the currently operational applications data stored in the ATC. .

Upload/Download Data Block(s) as needed to Transfer Files and Accommodate Bulk Transfers of new Application Databases

This feature allows an operator to remotely or locally download or upload complete data blocks or data files from another computer device. It supports the operator's ability to do bulk transfers of complete application databases to and from the ATC.

Monitor and Verify Present Applications Status

This feature allows an operator to remotely or locally view real-time reports of current applications status. The feature, depending on the application, would allow the operator to view status indicators such as operating modes, failure status, event logs, operation algorithm outputs, etc.

Allow Operator Control Application Execution (start/stop/run time/etc.)

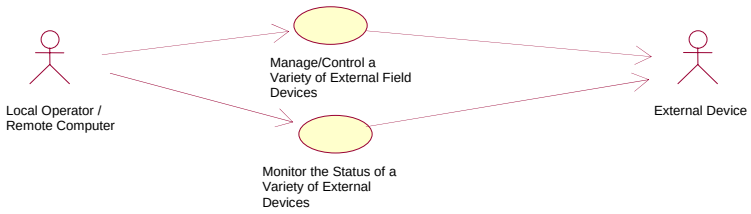
This feature allows the operator to manage the starting, stopping, and scheduling of one or more applications on the ATC.

Facilitate the Long Term Storage of Data for Logging and other Data Storage Applications

This feature facilitates the long storage of data for logging and other data storage applications

Manage External Devices

The various sub-features for “managing external devices” are shown in the following figure. The subsequent sections detail these subfeatures.



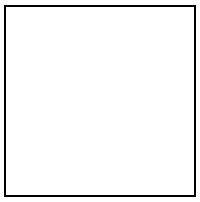


Figure 0-6: ‘Manage External Devices’ Subfeature Areas

Manage/Control a Variety of External Field Devices

This feature addresses the need for devices to be controlled both remotely (from a central computer) and locally (either from the controller directly or from a laptop computer connected to the controller).

Monitor the Status of a Variety of External Field Devices

This feature provides the capability for the controller to monitor device status and to use that status for local control conformation, failure diagnosis, logging and/or reporting to a local operator or remote computer.

Facilitate ease of maintenance & future hardware and software updates

The various sub-features for "facilitating ease of maintenance & future hardware and software" are shown in the following figure. The subsequent sections detail these subfeatures.

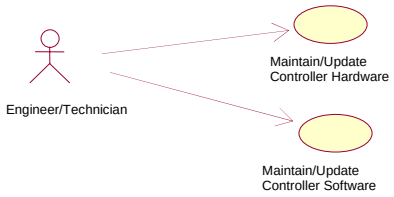


Figure 0-7: 'Facilitate ease of maintenance & future hardware and software updates' Subfeature Areas

Maintain/Update Controller Hardware

This feature addresses the need for controller unit hardware to be maintained and updated as technology changes and additional functional and performance capabilities are needed.

Maintain/Update Controller Software

This feature addresses the need for controller applications software to easily be maintained, updated, or ported between different manufacturer's hardware units.

2.7 Security

The standard does not address security issues. Any security should be implemented in by the application software hosted by the ATC or physically by protecting access to the ATC and its interfaces.

2.8 Modes of Operation

The features identified above were developed with these three modes of operation in mind. These modes include “standalone”, “direct” and “distributed” as described below. Doesn’t the application software primarily define this? Is this a standard for the hardware or software? Why would the hardware configuration care about this?

The “standalone” control mode assumes that the ATC is operating in the field without remote monitoring by a central computer or master controller. In this mode, applications software is loaded into non-volatile controller memory and used to control and/or monitor externally connected devices such as gates, signals, beacons, signs, etc. Device control is based on locally stored schedule, predefined control algorithms or manual operation by person present at the controller. Device monitoring might include processing of remote sensor inputs and/or monitoring the results of the controller’s control actions. Under this mode, no communications is assumed to exist between the ATC and central computer or remote master. Local operator interactions take place through ATC front panel interface, laptop computer, or similar portable device.

The “direct” control mode assumes that a remote control center or master device directly controls the external device(s) connected to the ATC. In this mode, commands are sent from control center/master to the ATC via communications network to affect the operation of local device(s) connected to the ATC.

The “distributed” control mode is a combination of the first two. Here the local ATC applications software exercises normal control but the operation is managed and synchronized through a communication network connection with a central computer or master. Control operations may frequently be overridden remotely to meet current needs and situations.

Section 3

ATC 3000 Controller Unit Functional Requirements

This section defines the Functional Requirements to be supported by the ATC 3000 based on common "use cases" identified in Section 2.

Following the Concept of Operations (see Section 2), the operation of the ATC 3000 has been categorized into three major areas:

- Manage/Configure Controller Applications
- Manage External Devices
- Facilitate Ease of Maintenance & Future Hardware or Software Updates

In the Concept of Operations, these major areas are each broken down into sub-items. This Functional Requirements section also follows this structure.

The ATC 3000 is fundamentally defined as a general purpose field computing device supporting many different possible software applications, therefore the particular functional and sub-functional requirements applicable to any particular implementation can not be fully defined here.

3. 1 Manage/Configure Controller Applications

a. Installing/Updating Applications Software Quickly and Efficiently

i. Locally – satisfied by the following requirements:

1. Front panel connected dedicated Serial port for interfacing with laptop computer, PDA or similar locally connected device with software for performing this function
2. Front panel connected dedicated Ethernet port for interfacing with laptop computer, PDA or similar locally connected device with software for performing this function
3. Front panel Memory device interface and a minimal front panel user interface for initiating bulk data transfers to and from a removable memory device – satisfied by following requirements:
    a. USB port with support for memory stick and API mechanism for memory device file access- This port could be the connection to a PDA.

b. Front panel display and keyboard or a serial interface for connection to connected Laptop computer or PDA device to serve as an operator interface for initialing file transfers to and from a memory stick device when such a device is connected to USB port per above requirement

ii. Remotely – satisfied by the following requirements:
   1. Separate dedicated Ethernet port for possible use to communicate with a remote computer device having the necessary software for performing this function.
   2. Separate dedicated Serial port for possible use to communicate with a remote computer device having the necessary software for performing this function.

b. Installing and Upgrading the Operating System Software (including drivers, applications programming interfaces, utilities, etc.)
   i. Locally – satisfied by supporting requirements listed under 3.1.a.i above.
   ii. Remotely – satisfied by support of requirements listed under 3.1.a.ii above.

c. Maintain Clock/Calendar Function and Synchronize with Reliable External Sources as needed – is supported by the following:
   i. This Controller shall include resident clock/calendar device to to transfer files support to the maintenance and backup of current time and date by the controller unit in the absence of AC power
      1. Clock/calendar device shall be capable maintain time/date for a minimum of 30days without AC power applied to the controller unit
      2. Clock/calendar device drift shall be less than xxx per day.
      3. Applications software executing in the controller unit shall be able to set time and date on the resident clock/calendar device to the nearest 1/10 sec via a standardized Applications Programming Interface (API)
   ii. When AC power is applied to the unit, a clock pulse derived from AC power source shall be monitored by the operating system for use in correcting current time for long term drift.
   iii. When AC power is present, current time/date information should be maintained by the operating system and easily accessed by controller resident application software utilizing a standardized Applications Programming Interface (API)

d. Configure and Verifying Parameter(s) - for particular local applications
   i. Locally – shall be supported by:
      1. Optional front panel display and keyboard(s) to support operator configuring/verifying of application parameter(s) and/or
      2. Dedicated serial communication port for locally connected laptop, PDA or similar device with software to support operator configuring/verifying application parameter(s) from this device
   ii. Remotely – shall be supported by:
      1. satisfied by support of requirements listed under 3.1.a.ii above, and
      2. presence of Application Programming Interface supporting NTCIP transfers through remote system interfaces

e. Uploading/Downloading Data Block(s) - as needed to transfer files and accommodate bulk transfers of new application databases
   i. Locally – supported by Communication port (as listed in 3.1.a.i above) for interface to locally connected laptop, PDA or similar device with necessary software to support operator configuring/verifying application parameter(s) from this device
   ii. Remotely – supported by:
      1. same requirements as listed under 3.1.a.ii above, and
      2. presence of Application Programming Interface supporting NTCIP transfers through remote system interfaces

f. Monitoring and Verifying Present Application Status - (overall health of system as well as internal parameters related to particular application such as operating modes, event logs, device failures, algorithm results, etc.)
   i. Locally – supported by Communication ports (as listed in I.a.i above) for interface to locally connected laptop, PDA or similar device with necessary software to support operator monitor and verifying of present applications status from this device
   ii. Remotely – supported by:
      1. same requirements as listed under 3.1.a.ii above, and
      2. presence of Application Programming Interface supporting NTCIP transfers through remote system interfaces

g. Allowing Operator Control of Application(s)- (start/stop/run time):

i. Locally – supported by:
   1. Communication ports (as listed in 3.1.a.i above) for interface to locally connected laptop, PDA or similar device with necessary software to support operator to control application control (start/stop/run time/etc.)
   2. presence Application Programming Interface allowing controller resident operator interface software to control other applications tasks (start/stop/run time/etc.)

ii. Remotely – not supported

h. Facilitate the Long Term Retention of Data - for logging and other local data storage applications

Supported by:
   1. flash memory for applications to store data
   2. API supported flash memory file management system

3.2 Manage External Devices

a. Monitor the Status of a Variety of External Field Devices – supported by providing interfaces that allow this controller to communicate to external devices via industry standard asynchronous and synchronous serial communications connections. Supported by:

i. Supported by a minimum of four (4) otherwise undedicated general purpose serial communications ports for possible interface to external field devices:
   1. each port shall support asynchronous and synchronous communications
   2. each port shall support a range of baud rates up to and including 56kb/sec asynchronous and 512kb/sec synchronous
   3. ports shall be configurable to RS232, RS422 or RS423 interface standards

ii. Provide packaging and interfaces that allow this controller to be deployed in industry standard cabinets configuration including: TS2 Type 1 & 2 cabinets, the ITS Cabinet and the 170 cabinets. (The controller must provide backward interface compatibility with existing NEMA, 170, and 2070 controllers
   1. A minimum of one dedicated synchronous serial port for interface to ITS Cabinet or TS2 Type 1 Cabinet (or optional interface modules described under II.c.ii and II.c.iii below).

2. Optional serial to parallel interface module for connection to TS2 type 2 cabinet.
3. Optional serial to parallel interface module for connection to Model 170 cabinet.
4. The Controller unit shall be packaged in a housing designed for both rack mount and shelf mount cabinet configurations. Why can't we retain different packages for each or an entirely new package such as might be used in a CBD type cabinet, which may simply be a single card.
    a. Units shall be capable of being mounting in a standard EIA 19" rack cabinet including, but not limited to, cabinets adhering to the new ITS Cabinet and the Caltrans 332 cabinet standards.
    b. Rack mounting hardware shall be optional for units purchased for shelf mounting but such units shall be capable of easily being retrofitted for rack mounting capability at a later date.
    c. All units shall be shelf mountable for operation in standard NEMA TS1, TS2 cabinet or similar configurations. But which "end/side" will have the connectors, front or back?
    d. Unit's dimensions shall be no greater than those of the current ATC 2070.

b. Manage/Control a Variety of External Field Devices -

- Supported by same ports described under 3.2.a above.

3.3 Facilitate Ease of Maintenance & Future Hardware or Software Updates

a. Provide support for a standardized Application Programming Interface (API) - to facilitate the porting of applications software between different CPU and operating systems combinations - API shall support, as a minimum the following classes of functions:
    i. Serial communications
    ii. Field cabinet I/O
    iii. Flash memory file management
    iv. Applications task control
    v. Time & date management functions
    vi. User interface support

b. Provide a Platform that allows easy field Hardware Upgrades - to adapt to newer processors, operating systems, and increased memory size and speed – provided by
    i. Requirement for a engine board module with:
        1. CPU and RAM memory
        2. Flash memory storage
        3. Operating System Software

4. All required serial ports
5. Ethernet interface
6. Standardized (form, fit and function) pin out interface

ii. The ATC 3000 CU shall optionally include a plug-in internal Communication Board module(s) adhering to:
    1. Standardized interface (form, fit, and function) established such that the Communication Boards of various manufacturers shall operate properly when installed within an another manufacturer's unit)
    2. If a Communications Board slot(s) is provided, slot(s) shall support current Communication Boards modules that adhere to the form, fit and electrical interface specifications of the ATC 2070 standard

Section 4
Engine Board Details

4.1 General Information

4.1.1. Engine Board

The Engine Board is the heart of an ATC-3000. The ATC-3000's processor, all memory devices, serial interface devices and processor housekeeping circuits will be located on the Engine Board, which will be interchangeable between manufacturers. The plug-in form factor and standardized connectorization of the Engine Board allow it to fit into a wide variety of host controllers to suit any particular application.

The Engine Board is designed as a modular unit with the following features and characteristics:

permits uniqueness of overall ATC-3000 hardware design while maintaining software compatibility and portability
provides a cost-effective migration path for future capability expansion
provides for interchangeability and innovation between manufacturers but not much!
facilitates customization of an ATC-3000 for particular applications

The Engine Board dramatically simplifies future updates of the processor, operating system, memory and other core elements of the ATC-3000.

These specifications for the Engine Board require a minimum level of real-time processing capability. Suitable software will also be specified in order to determine whether a proposed Engine Board meets the minimum requirements. Manufacturers are free to add additional capabilities to their Engine Board designs so long as said functionality does not conflict with this specification in any way.

Guidance: There has been much discussion and debate regarding the approach taken in this document regarding the ATC-3000 Engine Board, in particular the obvious ties to the ATC-2070. The consensus of the Project Team from the beginning has been that this work should represent an evolution of that design, rather than a revolutionary new design, and should build upon and enhance the strengths of that design while addressing the shortcomings which prevent the ATC-2070 from adequately meeting current and future requirements as outlined in this document. But this Engine Board itself is a new design, far newer than PC104.

The following concepts were the fundamental basis upon which the functional and design requirements specified herein for the Engine Board have been established:

Build on the CPU platform already specified by the ATC-2070. I don't know if there is universal agreement on this.

Encapsulate the CPU-specific elements (processor/support hardware/OS) into a modular form which will provide a reliable migration path for future performance and obsolescence upgrades.
Update existing features of the CPU functionality to make better use of current technology.
Selectively add new features, which may now be available through advancements in technology, only where said features are necessary in order to meet designated functional requirements.
Reference the upcoming ATC API for much of the detailed operational requirements.

4.1.2. Engine Board Host

The Engine Board Host shall provide the mechanical and electrical interface to the Engine Board, and is responsible for providing sufficient power and interface paths as required by this specification. With the exception of these requirements, which are detailed in this specification, manufacturers are free to construct virtually any type and form of ATC-3000 host to meet any specific market need.

4.2 Mechanical and Physical

Board Dimensions and Mechanical Requirements

The maximum dimensions of the Engine Board shall be 5.00” L x 4.00” W x 1.087” D. The nominal thickness of the PCB material shall be 0.062".

The Engine Board shall have two interface connectors and four standoff holes, which shall be located as illustrated in Figure 1. Each connector shall have fifty pins, numbered 1-50, beginning with pin number 1 as the upper left-hand pin on each connector and with pin numbers increasing left-to-right and top-to-bottom. Standoff holes and the spacing around them shall be sized to accommodate a standard 4-40 Phillips pan-head screw. Standoffs and/or captive fasteners are not required to be used, however the Engine Board must meet all environmental specifications regarding vibration and shock utilizing the manufacturer's standard mounting technique.

Components may be placed on either side of the printed circuit board (PCB). Component height, with the exception of the interface connectors, shall not exceed 0.325” on the bottom (connector side) of the PCB and shall not exceed 0.600” on the top side of the PCB.

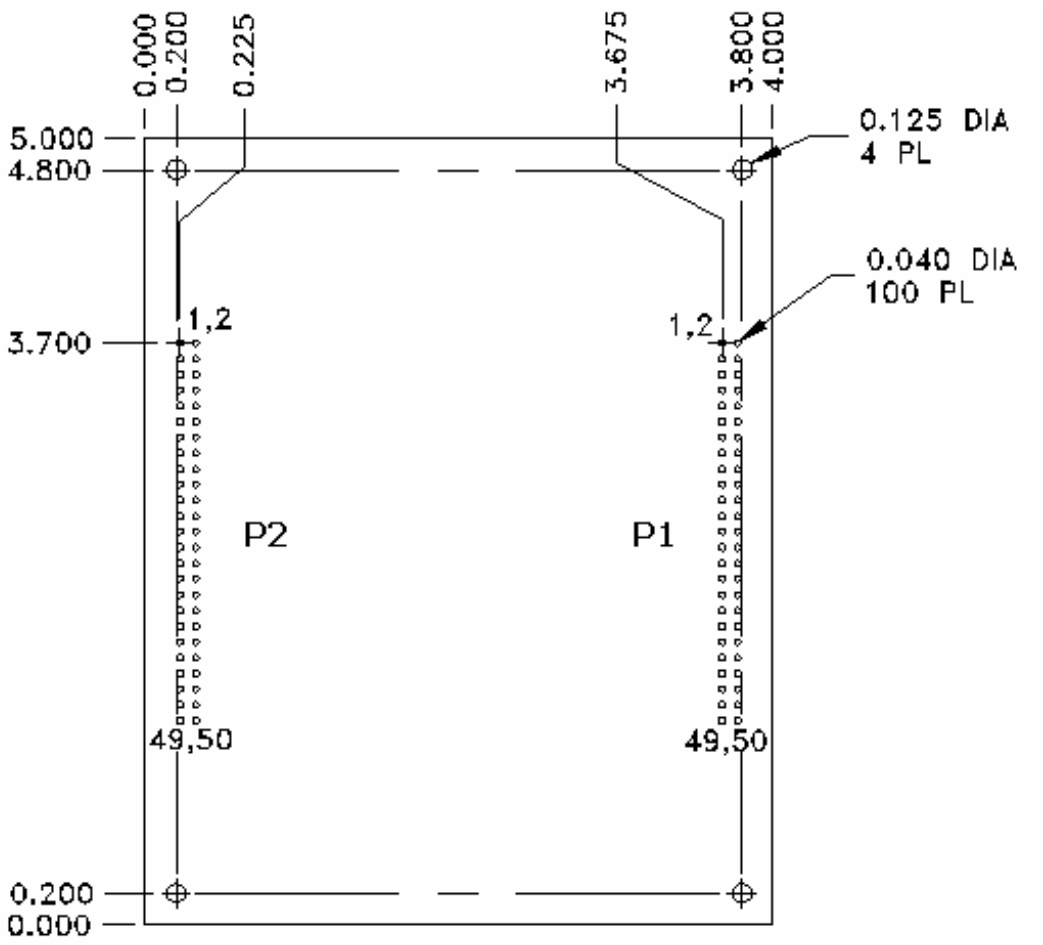


Figure 1 - Engine Board Top View What about a side view?

Connector Pinout and Signal Names

The Engine Board shall have two connectors, designated P1 and P2, which are mounted on the bottom of the PCB. These connectors shall be dual-row, low-profile headers with the following specifications:
Turn this stuff into a table so it is always in alignment.

distance post-to-post, same row:	0.100" nominal
distance post-to-post, between rows:	0.100" nominal
post size:	0.025" sq. nominal
insulator thickness:	0.060" +- 20%
post length:	0.280" minimum, 0.350" maximum
tail length (through PCB):	0.100" minimum, 0.150" maximum
post plating:	gold, 10u" minimum
representative part:	Samtec MTLW-125-07-G-D-07

Figure 2 lists the connector pinouts and signal names. All name designations are from the perspective of the Engine Board (for example, TXD means data transmitted by the Engine Board).

Figure 2 - Connector Pinout and Signal Names

Connector P1	Connector P2
VPRIMARY	VSTANDBY_5
VPRIMARY	VSTANDBY_3
VPRIMARY	RESERVED
VPRIMARY	RESERVED
GROUND	SP2_TXD
GROUND	SP2_RXD
GROUND	SP2_RTS
GROUND	SP2_CTS
SP1_TXD	SP2_CD
SP1_RXD	SP2_TXC_INT
SP1_RTS	SP2_TXC_EXT
SP1_CTS	SP2_RXC_EXT
SP1_CD	SP5_TXD
SP1_TXC_INT	SP5_RXD
SP1_TXC_EXT	SP5_TXC_INT
SP1_RXC_EXT	SP5_RXC_EXT
SP3_TXD	KEYING_PIN
SP3_RXD	RESERVED
SP3_RTS	USB_DPLUS
SP3_CTS	USB_DMINUS
SP3_CD	SP8_TXD
SP3_TXC_INT	SP8_RXD
SP3_TXC_EXT	SP8_RTS
SP3_RXC_EXT	SP8_CTS
SP4_TXD	SP8_CD
SP4_RXD	SP8_TXC_INT
SP6_TXD	SP8_RXC_EXT
SP6_RXD	CPU_RESET
CPU_ACTIVE	LINESYNC
ENET_TX_POS	POWERDOWN
ENET_TX_NEG	POWERUP
ENET_RX_POS	SPI_MOSI
ENET_RX_NEG	SPI_MISO
ENET_LED_TXD	SPI_CLK
ENET_LED_RXD	SPI_SEL_1
ENET_LED_CLSN	SPI_SEL_2
ENET_LED_LINK	SPI_SEL_3
SYSCLK_DIV_4	SPI_SEL_4
RESERVED	RESERVED
RESERVED	RESERVED
RESERVED	RESERVED
RESERVED	RESERVED
RESERVED	RESERVED
RESERVED	PROG_TEST
RESERVED	PROG_TEST
RESERVED	PROG_TEST
PROG_TEST	PROG_TEST
PROG_TEST	PROG_TEST
PROG_TEST	PROG_TEST
PROG_TEST	PROG_TEST

Environmental Requirements

Engine boards must meet all ATC-3000 environmental requirements per the ATC-3000 Controller Environmental Specification. Testing shall be performed with the Engine Board mounted in a suitable host controller assembly. The Engine Board shall be mounted using the same construction and retention devices used in the manufacturer's normal production. Would auxiliary cooling devices be allowed?

On-Board Resources

Central Processing Unit

The Engine Board shall incorporate a Central Processing Unit and support circuitry that shall have a minimum computational capability of 200 MIPS calculated using the Dhrystone v2.1 benchmark at 25°C. How much degradation is allowed at the environmental extremes? Is Dhrystone the correct benchmark for this application?

Startup Considerations

The Engine Board low-level hardware and operating system software initialization shall be complete and fully ready to load and execute application code within a maximum of 5.0 seconds from the initial application of DC power (VPRIMARY).
The Engine Board shall provide circuitry to prevent writing to the SRAM area and to keep the processor in a RESET state any time that VPRIMARY is less than the minimum-specified operating voltage regardless of the state of the POWERUP or POWERDOWN signals.

Memory

FLASH Memory

The Engine Board FLASH memory devices provide for the storage of operating system software and user application programs. A minimum of 6MB of FLASH memory shall be provided for use by application programs. Flash devices shall use a segmented architecture allowing erasing, writing and reading of individual segments. Any width of FLASH memory is acceptable, subject to any and all other performance requirements herein.

RAM Memory

Dynamic RAM (DRAM)

The Engine Board shall contain a minimum of 16MB of DRAM memory for program execution. This memory shall be organized in the native word length of the Engine Board processor for maximum performance and shall operate with zero wait states.

Static RAM (SRAM)

The Engine Board shall contain a minimum of 1MB of SRAM memory for non-volatile parameter storage. This memory shall be organized in at least half of the native word length of the Engine Board processor. In the absence of primary Engine Board power VPRIMARY the SRAM shall be supported and maintained by one of the standby power sources VSTANDBY_5 or VSTANDBY_3. Current drawn from the standby power source shall not exceed 200 uA at 25°C.

Real-Time Clock (RTC)

A software-settable, hardware Real-Time Clock (RTC) shall be provided. The clock shall track seconds, minutes, hours, day of month, month and year. In the absence of primary Engine Board power VPRIMARY the RTC shall operate from one of the standby power sources VSTANDBY_5 or VSTANDBY_3 and shall maintain an accuracy of +-0.005% per 30 days at 25°C. Current drawn from the standby power source shall not exceed 25 uA at 25°C.

Guidance: It is expected and understood that the controller's RTC and internal software clock will need to be periodically resynchronized with an external source, either via system communications or by a local WWVB or GPS receiver connected serially.
The system drawing should detail the port where this connection should be made. But it should also not rule out GPS chipset on the engine board itself.

ATC-3000 API Support

The ATC-3000 API Specification provides for a standardized Application Programming Interface (API) in support of all hardware features and functionality of the Engine Board as well as other controller components and modules. All Engine Board components, including but not limited to the processor, all memory components and support circuitry, must be capable of providing the required functionality in its entirety as defined by the ATC-3000 API.

Electrical Interface

Power

Operating Voltages and Currents

Primary power shall be applied to the Engine Board between the VPRIMARY and GROUND interface pins. The Engine Board shall be capable of operation from any supply voltage ranging from +4.8VDC to +5.2VDC on the VPRIMARY supply. The power requirement shall not exceed 10.0 Watts from the VPRIMARY supply.

All Engine Board interface pins defined as logic-level inputs must be 5V tolerant.

Any additional voltages required for normal operation by the Engine Board, such as 3.3VDC, shall be derived from primary power VPRIMARY by circuitry located on the Engine Board.

The Engine Board is not required to provide standby power in support of the SRAM or RTC. In the absence of primary Engine Board power VPRIMARY these components shall be supported and maintained by one of the standby power sources VSTANDBY_5 or VSTANDBY_3 provided by the Engine Board Host interface. VSTANDBY_5 shall provide standby power to the Engine Board at 5.0VDC ± 10%. VSTANDBY_3 shall provide standby power at 3.3VDC ± 10%. A total of 225 uA may be drawn from both standby sources. VSTANDBY_5 and VSTANDBY_3 may be sourced from the same backup power storage device on the host interface, and the total current requirement is considered to be shared between the two sources.

PCB Layout Considerations

The Engine Board connectorization provides point-source introduction of power and ground from the ATC-3000 host in order to minimize power and ground loops. The Engine Board PCB layout shall be performed in such a manner so as to provide the most reliable and robust power distribution possible to the individual board components. Individual power and ground planes shall be provided for VPRIMARY and GROUND. No signal traces, other than VPRIMARY and GROUND, shall appear on these two plane layers. At least 90uF of low-ESR bulk capacitance shall be provided on the Engine Board across VPRIMARY and GROUND. Despiking capacitors across VPRIMARY and GROUND shall be used liberally, particularly adjacent to those components which operate at or near the processor's bus speed.

Power Interruption and Restoration

The Engine Board must properly interpret and respond to power control signals provided by the ATC-3000 host, specifically the POWERUP and POWERDOWN signals.

The Engine Board shall provide circuitry to prevent writing to the SRAM area and to keep the processor in a RESET state any time that VPRIMARY is less than the minimum-specified operating voltage regardless of the state of the POWERUP and POWERDOWN signals.

POWERUP

POWERUP is a logic-level input signal to the Engine Board. This input signal is normally in the HIGH state following a controller cold start and during normal operation. A HIGH-to-LOW transition, while the POWERDOWN signal is also in the LOW state, indicates to the Engine Board that a cold restart is to be performed. This condition is considered a long power outage. A HIGH-to-LOW transition while the POWERDOWN signal is in the HIGH state should be ignored.

POWERDOWN

POWERDOWN is a logic-level input signal to the Engine Board. This input signal is normally in the HIGH state following a controller cold start and during normal operation. A HIGH-to-LOW transition indicates to the Engine Board that AC power to the controller has been lost. This signal serves as an advance warning of an impending power failure, and can be used to trigger data storage or other pre-shutdown activities. Should the POWERDOWN signal transition from LOW-to-HIGH with the POWERUP signal in the HIGH state, the Engine Board application software shall continue operating normally without a restart. This condition is considered a short power outage.

Synchronization

LINESYNC

The LINESYNC signal is an input to the Engine Board and provides a 50% duty cycle square-wave at 60Hz. This signal is at logic-level between VPRIMARY and GROUND, and is used to provide a periodic interrupt to the Engine Board processor for use as a system tick reference. This signal must be monitored and used according to the requirements defined by the ATC-3000 API.

Serial Interface Ports

Serial Communications Interface Ports

The Engine Board shall provide seven serial communications ports. These ports are described below. Each port shall be capable of operating at a completely independent bit rate from all other ports. Default bit rates are indicated by (*). All interface pins shall be at logic-levels. Input pins are indicated by (I), output pins by (O).

There are way too many serial ports. The majority of the ports don’t appear to serve much purpose. For example I could cross connect the outputs for the “Communications

Interface Connector to the TTL to Serial Interface Link to Modem devices and talk to my self?

Serial Port 1 (SP1)

Principal Usage:	general-purpose
Operating Modes:	ASYNC / SYNC / HDLC / SDLC
Asynchronous Rates (bps):	(*)1200 / 2400 / 4800 / 9600 / 19.2k / 38.4k / 57.6k / 115.2k
Synchronous Rates (bps):	(*)19.2k / 38.4k / 57.6k / 76.8k ??? repeat/ 153.6k
Interface Pins:	SP1_TXD: Transmit Data (O)
SP1_RXD:	Receive Data (I)
SP1_RTS:	Request To Send (O)
SP1_CTS:	Clear To Send (I)
SP1_CD:	Carrier Detect (I)
SP1_TXC_INT:	Transmit Clock Internal (O)
SP1_TXC_EXT:	Transmit Clock External (I)
SP1_RXC_EXT:	Receive Clock External (I)

Serial Port 2 (SP2)

Principal Usage:	general-purpose
Operating Modes:	ASYNC / SYNC / HDLC / SDLC
Asynchronous Rates (bps):	(*)1200 / 2400 / 4800 / 9600 / 19.2k / 38.4k / 57.6k / 115.2k
Synchronous Rates (bps):	(*)19.2k / 38.4k / 57.6k / 76.8k / 76.8k repeat???? / 153.6k
Interface Pins:	SP2_TXD: Transmit Data (O)
SP2_RXD:	Receive Data (I)
SP2_RTS:	Request To Send (O)
SP2_CTS:	Clear To Send (I)
SP2_CD:	Carrier Detect (I)
SP2_TXC_INT:	Transmit Clock Internal (O)
SP2_TXC_EXT:	Transmit Clock External (I)
SP2_RXC_EXT:	Receive Clock External (I)

Serial Port 3 (SP3)

Principal Usage:	in-cabinet communications
Operating Modes:	ASYNC / SYNC / HDLC / SDLC
Asynchronous Rates (bps):	(*)1200 / 2400 / 4800 / 9600 / 19.2k / 38.4k / 57.6k / 115.2k
Synchronous Rates (bps):	153.6k / (*)614.4k
Interface Pins:	SP3_TXD: Transmit Data (O)
SP3_RXD:	Receive Data (I)
SP3_RTS:	Request To Send (O)
SP3_CTS:	Clear To Send (I)
SP3_CD:	Carrier Detect (I)
SP3_TXC_INT:	Transmit Clock Internal (O)
SP3_TXC_EXT:	Transmit Clock External (I)
SP3_RXC_EXT:	Receive Clock External (I)

Serial Port 4 (SP4)

Principal Usage:	external user-interface (console)
Operating Modes:	ASYNC
Asynchronous Rates (bps):	1200 / 2400 / 4800 / (*)9600 / 19.2k / 38.4k / 57.6k / 115.2k
Interface Pins:	SP4_TXD: Transmit Data (O)
SP4_RXD:	Receive Data (I)

Serial Port 5 (SP5)

Principal Usage:	SDLC to FIO and/or in-cabinet devices
Operating Modes:	ASYNC / SYNC / HDLC / SDLC
Asynchronous Rates (bps):	1200 / 2400 / 4800 / (*)9600 / 19.2k / 38.4k / 57.6k / 115.2k
Synchronous Rates (bps):	153.6k / (*)614.4k
Interface Pins:	SP5_TXD: Transmit Data (O)
SP5_RXD:	Receive Data (I)
SP5_TXC_INT:	Transmit Clock Internal (O)
SP5_RXC_EXT:	Receive Clock External (I)

Serial Port 6 (SP6)

Principal Usage:	front panel user-interface
Operating Modes:	ASYNC

Asynchronous Rates (bps):	1200 / 2400 / 4800 / 9600 / 19.2k / (*)38.4k / 57.6k / 115.2k
Interface Pins:	SP6_TXD: Transmit Data (O)
SP6_RXD:	Receive Data (I)

Serial Port 7 (SP7)

Principal Usage:	general-purpose
Operating Modes:	ASYNC / SYNC / HDLC / SDLC
Asynchronous Rates (bps):	(*)1200 / 2400 / 4800 / 9600 / 19.2k / 38.4k / 57.6k / 115.2k
Synchronous Rates (bps):	(*)19.2k / 38.4k / 57.6k / 76.8k / 76.8k repeat ?????/ 153.6k
Interface Pins:	SP8_TXD: Transmit Data (O)
SP8_RXD:	Receive Data (I)
SP8_RTS:	Request To Send (O)
SP8_CTS:	Clear To Send (I)
SP8_CD:	Carrier Detect (I)
SP8_TXC_INT:	Transmit Clock Internal (O)
SP8_RXC_EXT:	Receive Clock External (I)

Serial Peripheral Interface Port

The Engine Board shall provide a synchronous Serial Peripheral Interface Port. All SPI interface pins shall be at logic-levels. Input pins are indicated by (I), output pins by (O).

The implementation of SPI_SEL_1 is required to support DataKey operations. The other select lines are currently unimplemented and are reserved for future SPI-related expansion.

Serial Peripheral Interface (SPI)

Principal Usage:	DataKey interface
Operating Modes:	SYNC
Synchronous Rates (bps):	(application-specific)
Interface Pins:	SPI_MOSI: Master-Out-Slave-In (O)
SPI_MISO:	Master-In-Slave-Out (I)
SPI_CLK:	Clock (O)
SPI_SEL_1:	Select 1 (O)
SPI_SEL_2:	Select 2 (O)
SPI_SEL_3:	Select 3 (O)
SPI_SEL_4:	Select 4 (O)

Universal Serial Bus (USB) Port

The Engine Board shall provide a Universal Serial Bus (USB) port. The purpose of this port is to provide a simpler alternative to a laptop for field use by service technicians. This port will facilitate the transfer of large data files to and from the controller through the use of USB-based FLASH memory devices.

The following minimum requirements for this port have been established:

The USB port, as a minimum, shall conform to the appropriate sections of the USB v1.1 specification for both hardware and software operation in order to support the required file transfer operations. USB v2.0 support is not required, but may be provided.
To facilitate the transfer of files between dissimilar equipment, all USB memory devices shall be capable of being formatted using the FAT16 file system. This provides for a maximum per-device storage capacity of 2GB (assuming 32kB clusters).

Specific operational requirements for file transfers via the USB port shall be dictated by the ATC-3000 API Specification.

Interface Pins:	USB_DPLUS: Data Line Positive (I/O)
USB_DMINUS:	Data Line Negative (I/O)

1

Ethernet Port

The Engine Board shall provide a single 10BASE-T or 100BASE-T Ethernet port which fully conforms to the applicable requirements of IEEE 802.3-2002. Each Engine Board must have a unique 48-bit MAC address. All components necessary to produce the Ethernet physical layer, including the magnetic interface module, shall be located on the Engine Board.

Guidance: The ATC Host Interface will provide auto-negotiation is the term used by the 802.3 standard capability in support of both 10BASE-T and 100BASE-T.

Ethernet Interface (ENET)

Principal Usage:	local and network communications
Operating Mode:	synchronous, Manchester-encoded, differential
Synchronous Rates (bps):	10M
Interface Pins:	ENET_TX_POS: Transmit Data Positive (O)
ENET_TX_NEG:	Transmit Data Negative (O)
ENET_RX_POS:	Receive Data Positive (I)
ENET_RX_NEG:	Receive Data Negative (I)

Indicator Drive Signals

The Engine Board shall provide the following active-low, open-collector output signals used to display the current status of the Ethernet port:

ENET_LED_LINK:	displays current link status, active = good link
ENET_LED_TXD:	displays active transmit status, active = transmitting
ENET_LED_RXD:	displays active receive status, active = receiving
ENET_LED_CLSN:	displays network collisions, active = collision detected

Each output signal must be capable of sinking at least 30 milliamps at up to +30VDC. A pull-up resistor shall NOT be provided for these signals by the Engine Board.

Programming/Test Port

A manufacturer-specific programming and test port shall be provided on the Engine Board. Interface pins available for this purpose are designated PROG_TEST. This port (or ports) may be used for programming and testing of any on-board device(s). Examples of this test port include JTAG, BDM, Boundary-Scan, custom CPLD programming, and proprietary In-Circuit FLASH programming. Manufacturers are free to designate these pins for these purposes in any configuration on special Engine Board test adapter hosts, however all mating PROG_TEST pins on normal ATC-3000 hosts shall be no-connects.

Miscellaneous

CPU_RESET

CPU_RESET is an active-low, open-collector output signal generated by the Engine Board. This signal shall be provided to reset other system devices and shall be accessible to application programs through the ATC-3000 API. This output must be capable of sinking at least 30 milliamps at +5VDC. This signal shall have an onboard pull-up resistor of at most 10K ohms to VPRIMARY. This signal is intended for resetting logic-level devices only.

CPU_ACTIVE

CPU_ACTIVE is an active-low, open-collector output signal generated by the Engine Board. This signal shall be provided to indicate an active Engine Board processor and shall be accessible to application programs through the ATC-3000 API. This output must be capable of sinking at least 30 milliamps at up to +30VDC. A pull-up resistor shall NOT be provided for this signal by the Engine Board.

A typical use for this signal is to drive a front-panel 'active' or 'health' LED.

SYSCLK_DIV_4

SYSCLK_DIV_4 is a logic-level output from the Engine Board. It shall provide a 50% duty cycle square-wave at 6.144 MHz. This signal provides a clock reference for use by other components on the Engine Board Host interface.

KEYING_PIN

The interface pin designated KEYING_PIN is used to prevent incorrect insertion of the Engine Board into the host and is to be completely removed from its connector on the Engine Board.

RESERVED

All pins marked as RESERVED are reserved for future enhancements to the Engine Board specification and are not to be used for any purpose. They shall be no-connects on both Engine Boards and Engine Board Hosts.

Shouldn't we define a standard way of loading the application software? Consider how there is essentially a standard method of loading PC software? I wouldn't want maintenance folks to have to have different hardware and software for loading applications in different manufactures controller. That procedure should be detailed here.

Section 5
Communication Interface Details

5.1 GENERAL DESCRIPTION

The Communications Interface performs the signal conditioning needed to adapt the ATC serial I/O to various transmission media, such as phone lines, radio and optical fiber.

This Communications Interface Specification Section includes the following:

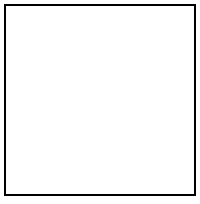
- **Transmission Media**
- **Modulation and Demodulation**
- **Mechanical Form Factor**

This Communications Interface Specification Section does not include the following:

- **Bit Rate Generation**
- **Data Content**
- **Error Detection and Indication**

This Communications Interface Specification allows the design and manufacture of hundreds of different varieties of communications modules, interchangeable among vendors. To meet this specification, a Communications Interface shall comply with:

- Mechanical dimensions and ATC connector of this specification
- Front panel connectors of this spec
- Modulation methods of this specific



4.1.1.1.1.1 CHOICE OF MEDIA

Standard Connectors For:
Private Line
Public Line, Dial-Up
Single Mode Fiber
Multi Mode Fiber

4.1.1.1.1.2 ATC STANDARD

This figure doesn't come acr

4.1.1.1.1.3 CHOICE OF MODULATION

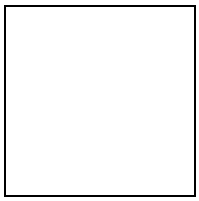
Frequency Shift Keying
Di Phase
ITU V.90
Optical Amplitude Modulation
Spread Spectrum
Bipolar Base Band
Balanced Differential Base Band

4.1.1.1.1.2.1 ATC Serial

5.2 MECHANICAL DESCRIPTION

5.2.1 Mechanical Outline Dimensions

The ATC Communications Interface uses the 2070 ATC A2 slot mechanical form factor and pin configuration. The mechanical dimensions are as follows:



5.2.2 ATC Connector Mechanical Pin Assignments

PIN	ROW A	ROW B	ROW C
1	SP1TXD+	SP6TXD+	SP5TXD+
2	SP1TXD-	SP6TXD-	SP5TXD-
3	SP1RXD+	SP6RXD+	SP5TXC+
4	SP1RXD-	SP6RXD-	SP5TXC-
5	SP1RTS+	SP1TXC0+	SP5RXD+
6	SP1RTS-	SP1TXC0-	SP5RXD-
7	SP1CTS+	SP1TXCI+	SP5RXC+
8	SP1CTS-	SP1TXCI-	SP5RXC-
9	SP1DCD+	SP1RXC+	SP3TXD+
10	SP1DCD-	SP1RXC-	SP3TXD-
11	SP2TXD+	SP4TXD+	SP3RXD+
12	SP2TXD-	SP4TXD-	SP3RXD-
13	SP2RXD+	SP4RXD+	SP3RTS+
14	SP2RXD-	SP4RXD-	SP3RTS-
15	SP2RTS+	SP2TXCO+	SP3CTS+
16	SP2RTS-	SP2TXCO-	SP3CTS-
17	SP2CTS+	SP2TXCI+	SP3DCD+
18	SP2CTS-	SP2TXCI-	SP3DCD-
19	SP2DCD+	SP2RXC+	SP3TXCO+
20	SP2DCD-	SP2RXC-	SP3TXCO-
21	DCGND1	NA	SP3TXCI+
22	NETWK1	NA	SP3TXCI-
23	NETWK2	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NETWK3	POWERUP	CPURESET
26	NETWK4	POWERDN	FPLED
27	DCGND1	DCGND1	DCGND1
28	+12 SER	-12 SER	+5 STDBY
29	+5 VDC	+5 VDC	+5 VDC
30	DCGND1	DCGND1	DCGND1
31	+12 VDC	+12 VDC	+12 VDC
32	DCGND2	DCGND2	DCGND2

Note:

Signal directions are referenced to the Engine Board, not the Communications Interface. For example, SP1TXD is Serial Port 1 data transmitted from the Engine Board to the Communications Interface. SP1RxD is Serial Port 1 data received by the Engine Board from the Communications Interface.

5.2.3 Mechanical Field Connections

5.2.3.1 EIA-232 Field Connections

EIA-232 field connection to the Communications Interface shall be via a 9-pin "D" connector (sockets) mounted on the Communications Interface front panel. The pin assignments are as follows:

Pin	*Signal*	*Description*	*Direction*
1	DCD	Carrier Detect	In
2	RxD	Received Data	In
3	TxD	Transmitted Data	Out
4	NA	Not Used	
5	DC GND	DC Reference	
6	NA	Not Used	
7	RTS	Request to Send	Out
8	CTS	Clear to Send	In
9	NA	Not Used	

5.2.3.2 EIA-485 Field Connections

EIA-485 field connections to the Communications Interface shall be via a choice of two connector arrangements:

5.2.3.2.1 One EIA-485 Port

EIA-485 field connection to 2 ports shall be via a 15-pin "D" connector (sockets) mounted on the Communications Interface front panel. The pin assignments are as follows:

Pin	*Description*	*Direction*
1	TxD+ Transmitted Data	Out
2	TxD- Transmitted Data	Out
3	RxD+ Received Data	In
4	RxD- Received Data	In
5	NA	
6	RTS+ Request to Send	Out
7	RTS- Request to Send	Out
8	CTS+ Clear to Send	In
9	CTS- Clear to Send	In

5.2.3.2.2 Two EIA-485 Ports

EIA-485 field connection to 2 ports shall be via a 15-pin "D" connector (sockets) mounted on the Communications Interface front panel. The pin assignments are as follows:

Pin	*Signal*	*Description*	*Direction*
1	TXDATA+	Transmitted Data	Out
2	DC GND	DC Reference	
3	TXCLOCK+	Transmitter Clock	Out
4	DC GND	DC Reference	
5	RXDATA+	Receiver Data	In
6	DC GND	DC Reference	
7	RXCLOCK+	Receiver Clock	In
8	NA	Not Used	
9	TXDATA-	Transmitted Data	Out
10	DC GND	DC Reference	
11	TXCLOCK-	Transmitter Clock	Out
12	DC GND	DC Reference	
13	RXDATA-	Receiver Clock	In
14	DC GND	DC Reference	
15	RXCLOCK-	Receiver Clock	In

5.2.3.3 Private Line Modulator / Demodulator (Modem) Connections

Private phone line twisted pair field connections to the Communications Interface shall be via a choice of two connector arrangements:

Internal and External Modem Connections

M14 AMP connector (sockets) mounted on the Communications Interface front panel. This connector includes signals for transmit twisted pair and receive twisted pair phone lines for use with internal modem, plus EIA-232 signals for use with external modem. The pin assignment is as follows:

Pin	*Signal*	*Description*	*Direction*
A	AUDIO IN	Phone Line Receive Pair	In (4 Wire)
B	AUDIO IN	Phone Line Receive Pair	In (4 Wire)
C	AUDIO OUT	Phone Line Transmit Pair	Out (4 Wire, I/O 2 Wire)
D	+5 VDC	Low Power +5 VDC Source	
E	AUDIO OUT	Phone Line Transmit Pair	Out (4 Wire, I/O 2 Wire)
F	NA		
H	DCD	Carrier Detect	In
J	RTS	Request to Send	Out
K	TXD	Transmitted Data	Out
L	RxD	Received Data	In
M	CTS	Clear to Send	In

N	DC GND	DC Reference
P	NA	
R	NA	

Internal Only Modem Connections

Nine pin "D" connector (pins) mounted to the Communications Interface front panel. This connector includes signals for transmit and receive twisted pair phone lines for use with internal modem. The pin out assignments are as follows:

Pin	*Signal*	*Description*	*Direction*
1	AUDIO OUT	Phone Line Transmit Pair	Out (4 Wire), I/O (2 Wire)
2	AUDIO OUT	Phone Line Transmit Pair	Out (4 Wire), I/O (2 Wire)
3	NA		
4	AUDIO IN	Phone Line Receive Pair	In (4 Wire Only)
5	AUDIO IN	Phone Line Receive Pair	In (4 Wire Only)
6	EQ GND		
7	NA		
8	NA		
9	EQ GND		

5.2.3.4 Dial-Up Line Modem Connections

Private phone line twisted pair field connections to the Communications Interface shall be via a 9 pin "D" connector (pins) mounted to the Communications Interface front panel. The pin assignments are as follows:

Pin	*Signal*	*Description*	*Direction*
1	NA		
2	NA		
3	NA		
4	NA		
5	NA		
6	EQ GND		
7	AUDIO I/O	Phone Line Pair	In / Out
8	AUDIO I/O	Phone Line Pair	In / Out
9	EQ GND		

5.2.3.5 Single Mode Fiber Connections

Single-mode fiber field connections to the Communications Interface shall be via 1300 nM threaded FC or 1300 nM ST connector for both laser transmitters and PIN diode receivers. What about 1550nm devices?

5.2.3.6 Multi Mode Fiber Connections

Multi-Mode fiber connections to the Communications Interface shall be via 820 nM ST connectors for both LED transmitters and phototransistor receivers. Multimode could also be 1310nM. But since this is not a specification for these devices do we care?

5.2.3.7 Wide Area Radio Connections

Wide area radio field connections to the antenna shall be via a TNC coaxial connector.

5.2.3.8 Infrared Connections

Wireless infrared field connections to an external device are via a red transparent window.

5.2.3.9. Ethernet Connections

Ethernet connections to the Communications Interface shall be via an RJ-45 modular jack, with the following pin configuration:

Pin	*Signal*	*Description*	*Direction*
1	TP	Transmitter Pair +	Out
2	TN	Transmitter Pair -	Out
3	RP	Receiver Pair +	In
4	NA		
5	NA		
6	RN	Receiver Pair -	In
7	NA		
8	NA		

5.3 OPERATIONAL DESCRIPTION

5.3.1 Interface to ATC

5.3.1.1 EIA-485 Signals

Except NETWORK1-NETWORK4 and FP LED, all signal lines of the 96-pin ATC connector shall be electrically EIA-485, balanced differential. Please refer to the EIA-485 document for electrical specifications.

The EIA-485 signals are biased by the ATC (not the Communications Interface Module) to provide the following:

- A 150 ohm resistor connected from DATA to /DATA on each simplex receiver.
- No termination resistor on each simplex transmitter
- A 150 ohm resistor connected from DATA to /DATA on each half duplex transceiver
- A 1.5K resistor from DATA to +5V and a 1.5K resistor from /DATA to DCGND1 to insure a stable state when the Communications Interface Module is not installed.

Please refer to the Communications Section for information on EIA-485 terminations.

5.3.1.2 Ethernet Signals

NETWORK1-NETWORK4 lines of the 96-pin ATC connector shall be 10 Base-T or 100 Base-T Ethernet. Proper selection of circuit board trace width, spacing, and shielding shall be observed for correct characteristic impedance and to prevent cross talk to adjacent signals.

5.3.1.3 Power Signals

DCGND1 shall be the common reference for +5 VDC, +12 SER, -12 SER and all signals.

DCGND2 shall be the common reference for +12 VDC.

5.3.1.4 Electrical Isolation

DCGND2 and +12 VDC as a group shall be electrically isolated from all other signals and power sources as a group, maintaining the isolation specifications of the Environmental Section. Eq GND shall maintain the isolation specifications of the Environmental Section.

Communications Interface field connections shall be electrically isolated from all ATC signals, power sources and EQ GND.

Field connections of the EIA-232 and EIA-485 versions of the Communications Interface shall be optically isolated using devices capable of at least 1 Mbps.

Field connections of the Ethernet, Private Line Modem and Dial-Up Modem versions of the Communications Interface shall be magnetically isolated via isolation transformers with the proper characteristic impedance.

Field connections of the Single Mode Fiber, Multi Mode Fiber and Infrared versions of the Communications Interface are inherently isolated via the non-conductive optical media.

Field connections of the Wide Area Radio version of the Communications Interface are inherently isolated via the non-conductive radio frequency media.

5.3.2 Modulation and Demodulation

5.3.2.1 EIA-232

(Guidance: This paragraph is intended to represent the present 2070-7A).

Description:

The EIA-232 versions of the Communications Interface shall convert the ATC EIA-485 signals to EIA-232 bipolar simplex, meaning each signal is unidirectional, point-to-point, without ability to disable the transmitter.
Indicators:

EIA-232 versions of the Communications Interface shall include the following indicators:

Front Panel Legend	Indicator Function
TX	ON= Transmitted Data at Field Wire is Positive Volts
RX	ON= Received Data at Field Wire is Positive Volts

Specifications:

Please refer to the EIA-232 specification for more detailed information on electrical specifications and signal definition.

5.3.2.2 EIA-485

(Guidance: This paragraph is intended to represent the present 2070-7B).

Description:

EIA-485 versions of the Communications Interface shall convert the ATC EIA-485 signals to isolated EIA-485, which may be simplex or half duplex.

Indicators:

EIA-485 versions of the Communications Interface shall include the following indicators:

Front Panel Legend	Indicator Function
TX	ON=DATA at Field Wire is 0V, /DATA at Field Wire is Positive Volts
RX	ON=DATA at Field Wire is 0V, /DATA at Field Wire is Positive Volts

Specifications:

Please refer to the EIA-485 specification for more detailed information on electrical specifications and signal definition.

5.3.2.3 Private Line Modem

Description:

Private Line Modem versions of the Communications Interface shall convert the ATC EIA-485 signals to modulated audio suitable for communications on an unconditioned private phone line pair, meaning the line is direct wire not connected to a phone company.

Modulation schemes used here convert the binary "1" and binary "0" bits of the data stream into audio tones, known as the MARK and SPACE. The demodulation scheme consists of converting each of the tones back to binary "1" and binary "0" bits to replicate the original transmitted data stream at the receiving device.

When RTS is asserted by the ATC, the modem shall transmit the MARK tone for a period of time, allowing the receiving modem to lock on to the tone and assert Carrier Detect (DCD). At the end of this time period, the transmitting modem asserts Clear to Send (CTS), signaling the ATC to begin sending data. At the end of the data packet, the ATC unasserts RTS and the transmitting modem stops sending a tone. DCD is unasserted by the receiving modem.

A front panel selector switch for each channel shall be provided to select FULL or HALF duplex operation. This scheme shall be capable of operating half-duplex on a single phone line, or full duplex on two different phone lines, one line for transmission and another line for reception, allowing simultaneous data transmission in both directions.

A second front panel selector switch for each channel shall disable the modem transmitter, in the event an ATC malfunctions with its RTS constantly asserted.

A third switch front panel shall break the power supply current to both channels, allowing the Communications Interface to be inserted into the ATC without causing a reboot or other ATC malfunction other than a normal recoverable communications error.

A fourth switch, mounted internally, shall implement anti-streaming which shall disable the modem transmitter in the event an ATC malfunctions with its RTS constantly asserted. If RTS is asserted for the specified time, the modem transmitter shall be turned OFF. The anti-streaming timer is reset if RTS is unasserted, or if TxD is active. This fourth switch allows anti-streaming to be disabled if the modem is installed in a FULL duplex central office, which continuously transmits to remote ATCs.

Indicators:

Front Panel Legend	Indicator Function
TX	ON= SPACE Tone at Field Wire
RX	ON= SPACE Tone at Field Wire
CD	ON= Received Tone Present

Modulation Methods:

Two different modulation methods shall be allowed under this specification as follows:

5.3.2.3.1 Frequency Shift Keying (FSK), 300 to 1200 bps, 0 to 9600 bps.

(Guidance: This paragraph is intended to represent the present 2070-6A and 2070-6B).

FSK modulation is simply transmitting one tone for a logic "1" (MARK) and a different tone for a logic "0" (SPACE), similar to pressing two different buttons on a touchtone telephone.

Two different FSK versions shall be available, which are 300 to 1,200 bps, as well as 0 to 9,600 bps. The two versions differ in the MARK and SPACE tones. The 0 to 9,600 bps version handles a wider variety of bit rates, but it's higher frequency tones travel shorter distances. For example, both versions transmit at the same power level and receive at the same sensitivity, but phone wire attenuates the higher frequencies of the 0 to 9600 bps version more rapidly. (Please refer to wire manufacturer's specifications for decibels (dB) loss per mile.)

Specifications:

The 300 to 1200 bps and 0 to 9600 bps shall have the following common specifications:

Modulation:	Phase coherent frequency shift keying (FSK).
Data Format:	Asynchronous, serial by bit.
Line:	Type 3002 voice-grade, unconditioned.
Transmit Level:	0 to –8 dB at 1.7 KHz, continuously adjustable
Sensitivity:	0 to –40 dB
Receiver Filter:	20 dB/Octave minimum active attenuation outside operating band
RTS to CTS Delay:	8 to 14 mS
Carrier Detect:	6 to 10 mS at MARK frequency
Receiver Squelch:	5.5 to 7.5 mS
Soft Carrier OFF:	8 to 12 mS
Recovery Time:	22 mS maximum from Transmit to Receive
Error Rate:	Less than 1 bit in 100,000 bits
Signal to Noise:	16 dB over 300 to 3000 Hz band
Transmit Noise:	-50 dB maximum into 600 ohms, 300 to 3000 Hz band
Anti-Stream Time:	6 to 8 seconds

The 300 to 1200 bps and 0 to 9600 bps specifications differ as follows:

	300 to 1200 bps Data Rate Version	0 to 9600 bps Data Rate Version
MARK Tone	1.2 KHz	11.4KHz
SPACE	2.2 K Hz	17.6KHz
Soft Carrier Freq	900 Hz	7.8 KHz

5.3.2.3.2 Di-Phase, 2,400 to 19,200 bps

(Guidance: This paragraph describes a modulation/demodulation technique to replace legacy 1200 bps FSK modems on existing unconditioned phone lines. Equivalent transmission distances are achieved at 19,200 bps, without software changes. ITU "V" series modems, such as V.90 are not recommended for this application due to the excessive RTS to CTS "training" time in half-duplex polling applications such as NTCIP.)

Di-phase modulation provides two tones as well as two phases, allowing increased bit rates over FSK modulation.

Specifications:

Modulation:	Differential Di-Phase, EUROCOM Standard D1
Data Format:	Asynchronous, serial by bit.
Line:	Type 3002 voice-grade, unconditioned.
Transmit Level:	0 to –8 dB at 1.7 KHz, continuously adjustable
Sensitivity:	0 to –40 dB
Receiver Filter:	20 dB/Octave minimum active attenuation outside operating band
RTS to CTS Delay:	8 to 14 mS
Carrier Detect:	6 to 10 mS at MARK frequency
Receiver Squelch:	5.5 to 7.5 mS
Soft Carrier OFF:	NA (no soft carrier)
Recovery Time:	22 mS maximum from Transmit to Receive
Error Rate:	Less than 1 bit in 100,000 bits
Signal to Noise:	16 dB over 300 to 3000 Hz band
Transmit Noise:	-50 dB maximum into 600 ohms, 300 to 3000 Hz band
Anti-Stream Time:	6 to 8 seconds

5.3.2.4 Dial Up Line Modem

(Guidance: This paragraph is intended to represent a standard dial-up modem.)

Description:

The Dial Up Modem versions of the Communications Interface shall convert the ATC EIA-485 signals to audio tones attached to public phone lines and switching equipment. The Dial Up Modem shall be capable of data transmission and reception, as well as dialing out and dialing in on a standard analog phone line.

Indicators:

Dial Up versions of the Communications Interface shall include the following indicators:

Front Panel Legend	Indicator Function
TX	ON= Transmitted Data Activity
RX	ON= Received Data Activity
CD	ON= Received Tone Present

RS	ON= RTS Asserted

Specifications:

Please refer to the ITU V.90 specification for detailed information on electrical specifications and signal definition.

5.3.2.5 Single Mode Fiber

(Guidance: This paragraph is intended to represent the 2070-6D.)

Description:

The Single Mode Fiber versions of the Communications Interface shall convert the ATC EIA-485 transmitted data to laser light, and laser light to ATC EIA-485 received data. Amplitude modulation (AM) is employed, meaning that a logic "0" is transmitted at a high light amplitude (or brightness), while logic "1" is transmitted at a lower (or OFF) amplitude.

Danger: Be aware that single-mode laser light is invisible to the human eye, but is of sufficient power to cause damage. Never look directly into a laser transmitter. Always cover unused laser transmitters with opaque dust covers.

Indicators:

Single Mode Fiber versions of the Communications Interface shall include the following indicators:

Front Panel Legend	Indicator Function
TX	ON= Transmitter is Emitting High Amplitude Light
RX	ON= Receiver is Detecting High Amplitude Light

Specifications:

Optical	1300 nM Single Mode Laser
Transmit Level:	-6 to –15 dBm, Continuously Adjustable
Receiver Sensitivity	-30 dBm
Data Rate	100K bps
Transmitter Compensation	Temperature and aging

5.3.2.6 Multi Mode Fiber

(Guidance: This paragraph is intended to represent the 2070-6D.)

Description:

The Multi Mode Fiber versions of the Communications Interface shall convert the ATC EIA-485 transmitted data to light, and light to ATC EIA-485 received data. Amplitude modulation (AM) is employed, meaning that a logic "0" is transmitted at a high light amplitude (or brightness), while logic "1" is transmitted at a lower (or OFF) amplitude.

Indicators:

Multi Mode Fiber versions of the Communications Interface shall include the following indicators:

Front Panel Legend	Indicator Function
TX	ON= Transmitter is Emitting High Amplitude Light
RX	ON= Receiver is Detecting High Amplitude Light

Specifications:

Optical	820 nM Multi Mode Light Emitting Diode (LED)
Transmit Level:	-6 to –15 dBm, Continuously Adjustable
Receiver Sensitivity	-30 dBm
Data Rate	100K bps
Transmitter Compensation	Uncompensated

5.3.2.7 Wide Area Radio

(Guidance: This paragraph is intended to represent a license-free data radio offering a good combination of distance and data integrity.)

Description:

The Wide Area Radio version of the Communications Interface shall convert the ATC EIA-485 transmitted data to RF, and RF to ATC EIA-485 received data. Spread spectrum frequency hopping is employed, meaning that the radio transmits at high power on a frequency channel, then "hops" to another channel. This insures that the average power transmitted on any one frequency is below the limit to require an FCC license.

Indicators:

Wide Area Radio versions of the Communications Interface shall include the following indicators:

Front Panel Legend	Indicator Function
TX	ON= Transmitted Data Activity
RX	ON= Received Data Activity

Specifications:

Radio Frequency Band	902 – 928 MHz Part 15 Spread Spectrum
Data Transmission	Simplex, Half Duplex and Full Duplex
Data Rate	1200 to 19,200 bps, Asychronous
Transmitter Power	1 Watt Maximum
Error Rate:	Less than 1 bit in 100,000 bits

5.3.2.8 Infrared

(Guidance: This paragraph is intended to represent an interface to a standard PDA.)

Description:

The Infrared versions of the Communications Interface shall convert the ATC EIA-485 transmitted data to light and light to ATC EIA-485 received data. The light beam is infrared, meaning it is outside the visible color range detected by the human eye. The light transmission is similar to a standard television remote control, meaning that its light emission power is safe to the human eye. As with a TV remote control, the transmitting device must be used within the line of sight, aimed towards the controller red window, and located within approximately six feet.

Indicators:

None

Specifications:

Optical	IrDA Physical Layer Implementation
Modulation	3/16 Encode / Decode
Data Rate	1200 bps to 115.2K bps

5.3.2.9 Ethernet

(Guidance: This paragraph is intended to represent the 2070-1B Ethernet)

Description:

The Ethernet version of the Communications Interface shall adapt the ATC NETWORK1-4 signals. The Ethernet port may be directly tied to NETWORK1-4 or buffered as a hub. This should be a switch not a hub. If there are other signals such as CCTV going thru this device it could easily over tax the Ethernet chip set on the CPU.

Indicators:

Due to the higher event speeds of Ethernet, each indication shall be extended 100 mS. Ethernet versions of the Communications Interface shall include the following indicators:

Front Panel Legend	Indicator Function
T	ON= Transmitted Data is logic "1"
R	ON= Received Data is logic "1"
C	ON= Collision of Data
L	ON= Link integrity good

Specifications:

Please refer to IEEE 802.3 for detailed specifications.

5.4 Communications Interface Versions

Each version of the Communications Interface shall consist of the following:

- A printed circuit board assembly of the size and shape described in Paragraph 2.1
- A connection to the ATC serial ports and power, as described in Paragraph 2.2
- One or more communications ports described in Paragraph 2.3
- Modulation / demodulation circuitry for each port, described in Paragraph 3.

By using different combinations of ports, an unlimited number of Communications Interface versions may be configured, compliant to this specification.

The following is a list of the existing Communications Interface Versions:

Part Number	Description
2070-6A	Dual 300 to 1200 bps Modem
2070-6B	Dual 0 to 9600 bps Modem
2070-6D	Fiberoptic Communications Interface
2070-7A	Dual EIA-232 Serial Interface
2070-7B	Dual EIA-485 Serial Interface

As new versions are defined, this list will expand.

Each version may be implemented using any of the following three design methods:

- Dedicated circuit design, each version ordered as separate vendor part numbers
- Common base board, with selectable modulation via plug-in circuit assemblies
- Common board, with selectable modulation via digital signal processor (DSP) software

Please refer to the Joint NEMA/AASHTO/ITE ATC Standard for detailed specifications of the 2070-6A, 2070-6B, 2070-7A and 2070-7B.

The Joint NEMA/AASHTO/ITE ATC Standard does not include a specification for the 2070-6D. The draft specification for the 2070-6D follows.

2070-6D Internal Fiber Modem

The 2070-6D Fiber Modem is a 1300 nM What about 1550? Single Mode fiberoptic transmitter and receiver. The 2070-6D provides two sets of fiber transmitter and receiver pairs that can operate as two independent serial channels (MASTER) or as a fiber repeater (REMOTE) via front panel switch selection. The 2070-6D incorporates powerful laser transmitters that provide high-speed data transmission at long distances.

2070-6D Operation

The 2070-6D Fiberoptic Converter is a printed circuit board assembly that plugs into the A2 slot of the 2070 ATC that is used to condition serial ports SP1 and SP2 for use with optical fiber, EIA-232, or EIA-485. The fiber cable attach to the 2070-6D via 1300 nM single mode fiber, FC style (what about SC and ST? or ???)threaded connectors But what protocols will this use, proprietary? You need to define the lower level protocols (coding) that this device must use. Can I buy anyone's 6D device and connect it to someone elses? Or must they be matched pairs? Is this a digital signal or an analog signal?

The 2070-6D has two front-panel switches. The MASTER/REMOTE switch selects whether the 2070-6D is installed in a Master Controller, or a Remote Controller, while the FIBER/DB9 switch enables or disables the DB9 connection to EIA-232 and EIA-485.

The 2070-6D contains internal rechargeable battery back-up circuitry that will power the fiber drivers and receivers for more than two hours after loss of controller power, preserving the integrity of the fiber link.

Operating Modes

The 2070-6D includes two 2-position front panel programming switches, resulting in four possible operating modes.

Master Mode 1: MASTER/REMOTE = MASTER, FIBER/DB9 = FIBER

This mode is used to drive two independent serial fiber links on two independent serial ports. In this mode, serial port SP1 transmits data on Emitter 1, and receives data on Detector 1. Serial port SP2 transmits data on Emitter 2, and receives data on Detector 2. In this mode, the DB9 connector is disabled.

Applications: This mode can be used to drive two separate fiber links, but is also commonly used to drive a single critical fiber ring (see Figure 1).

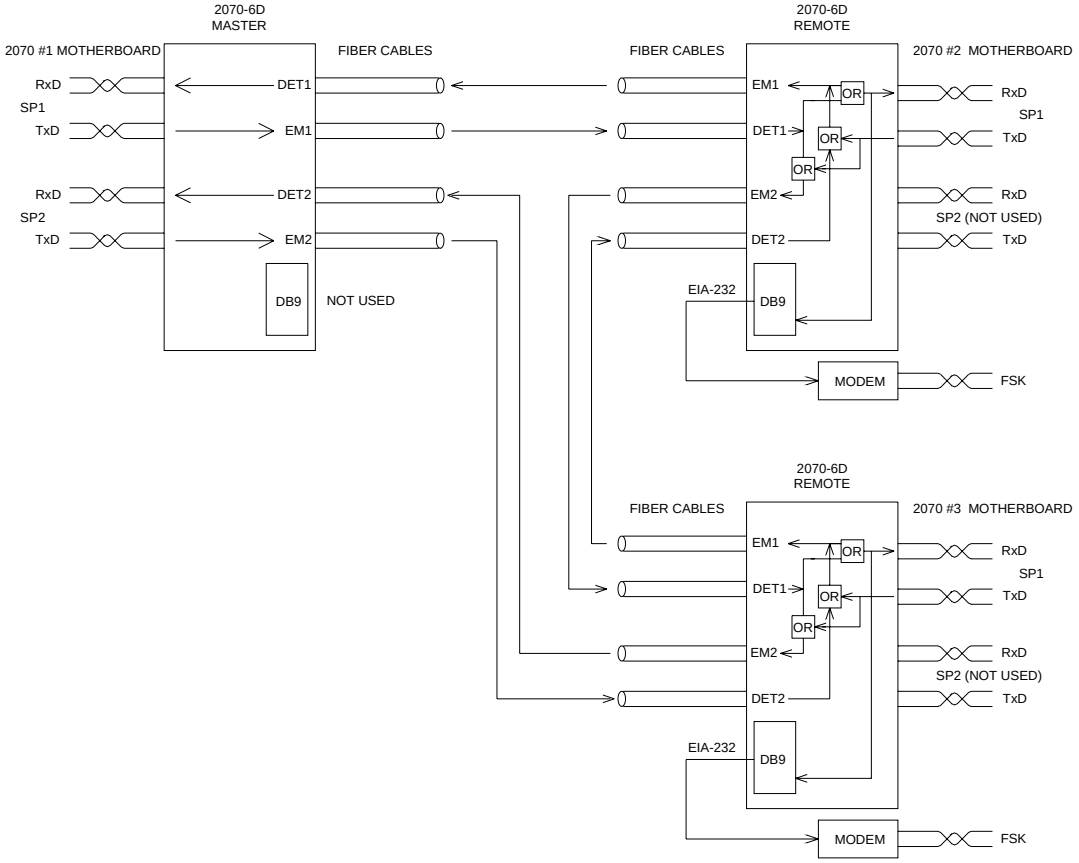


Figure 1: Master Mode 1 and Remote Mode 1

Master Mode 2: MASTER/REMOTE = MASTER, FIBER/DB9 = DB9

This mode is used to drive two fiber links simultaneously from one serial port, plus a hardwired serial link from a second serial port via the DB9 connector. In this mode, serial port SP1 transmits data simultaneously on Emitter 1 and Emitter 2. Data received on SP1 is the logical "OR" of Detector 1 and Detector 2. SP2 data is transmitted and received on the DB9 connector. The DB9 electrical characteristics conform to EIA-232 if SW1, section 1 is ON. The DB9 electrical characteristics conform to EIA-485 if SW1, section 1 is OFF.

Applications: This mode can be used to when the Master Controller is located in the center of a fiber link on SP1. The second serial channel (SP2) is a general purpose EIA-232 or EIA-485 serial channel to other devices.

Remote Mode 1: MASTER/REMOTE = REMOTE, FIBER/DB9 = DB9

This mode acts as a fiber signal booster/repeater on one serial port, plus a hardwired serial link from a second serial port via the DB9 connector. In this mode, data received on Detector 1 is received on serial port SP1 and also retransmitted simultaneously on Emitter 2. Data transmitted on Emitter 1 is the logical "OR" of data received on Detector 2 and data transmitted by SP1. Circuitry is provided to arbitrate collisions. If SP1 is already transmitting data on Emitter 1, data received on Detector 2 is locked out as long as SP1 Request to Send (RTS) is asserted. If data is already being retransmitted from Detector 2 to Emitter 1, SP1 Clear to Send (CTS) is asserted during, and for a short time after, the Detector 2 data. The duration of the CTS delay is either 1 mS or 10 mS after the end of the Detector 2 data. This delay is 1 mS if SW1, section 2 is ON. This delay is 10 mS if SW1, section 2 is OFF. The 10 mS delay is recommended for use with baud rates of 9600 or less. The 1 mS delay can be used for higher baud rates. SP2 data is transmitted and received on the DB9 connector. The DB9 electrical characteristics conform to EIA-232 if SW1, section 1 is ON. The DB9 electrical characteristics conform to EIA-485 if SW1, section 1 is OFF.

Applications: This mode is used to communicate with Remote Controllers via SP1, while boosting the optical signal to the next fiber link. The second serial channel (SP2) is a general purpose EIA-232 or EIA-485 serial channel to other devices (Figure 1).

Remote Mode 2: MASTER/REMOTE = REMOTE, FIBER/DB9 = FIBER

This mode is reserved for future use. The DB9, Emitters and Detectors are disabled.

Anti Streaming

Anti streaming prevents a serial channel from accidentally stalling and locking-up a serial channel. The anti streaming circuit constantly monitors the RTS output of each serial channel. If a serial channel stalls in transmit mode for seven seconds, the CTS input to that channel is unasserted, which takes that channel off-line. The anti streaming circuit continues hold CTS unasserted until RTS is unasserted, whereupon the 7-second anti streaming timer is reset. Anti streaming is enabled when SW4 section 3 is ON. Anti streaming is disabled when SW4 section 3 is OFF. Anti streaming is recommended except for long data streams, such as long uploads or downloads. Long data streams must be broken up into smaller packets if anti streaming is enabled.

Battery Back Up

The 2070-6D includes internal lithium rechargeable batteries that will power the fiber links for at least two hours upon the loss of power to the controller. The front panel includes a lamp labeled "CHARGED" which illuminates when the batteries are charged to full capacity.

Fiber Drivers

One fiber driver consists of EM1. A potentiometer is used to adjust the light output amplitude. The second fiber driver consists of EM2 and a second potentiometer, and operates in a similar fashion. Front panel lamps EM1 and EM2 are provided to indicate the state of EM1 and EM2 fiber drivers.

DANGER: NEVER LOOK INTO THE FIBER DRIVERS. THE LASER LIGHT IS INVISIBLE TO THE HUMAN EYE, BUT CAN CAUSE EYE DAMAGE. BE AWARE THAT EM1 AND EM2 CAN BE TRANSMITTING UNDER BATTERY POWER, EVEN WHEN THE CONTROLLER IS NOT POWERED, OR EVEN WHEN THE MODULE IS UNPLUGGED. FOR VISUAL STATUS, ALWAYS USE THE FRONT PANEL LAMPS, NOT THE FIBER CONNECTORS.

Fiber Receivers

One fiber receiver consists of DET1, while the second fiber receiver consists of DET2. Front panel lamps DET1 and DET2 provide visual status for each of the fiber receivers.

DB9 Communications

J1 is used for the DB9 communications. J1 is programmed by a DIP switch on the 2070-6D, to follow either EIA-232 or EIA-485 electrical standard.

Battery and Charger

All of the 2070-6D communications circuitry is powered by battery voltage to insure the fiber link remains powered. When the batteries are fully discharged, the regulator is shut down, preventing further discharge of the batteries. The 2070-6D contains a charge timer. If the battery does not fully charge within the specified time, the battery charger is turned OFF to prevent overheating.

Connectors

When programmed for EIA-232 operation, DB9 connector has the following pins:

Pin	Description	Direction
1	DCD Carrier Detect	Input
2	RxD Received Data	Input
3	TxD Transmitted Data	Output
4	No Connection	
5	DC Ground 1	
6	No Connection	
7	RTS Request to Send	Output
8	CTS Clear to Send	Input
9	No Connection	

When programmed for EIA-485 operation, DB9 connector has the following pin out:

Pin	Description	Direction
1	TxD+ Transmitted Data	Output
2	TxD- Transmitted Data	Output
3	RxD+ Received Data	Input
4	RxD- Received Data	Input
5	DC Ground 1	
6	RTS+ Request to Send	Output
7	RTS- Request to Send	Output
8	CTS+ Clear to Send	Input
9	CTS- Clear to Send	Input

Specifications

Item	Description	Min	Typ	Max	Units
Ts	Storage Temperature, non-operational	-40		85	C
To	Operating Temperature	-34	7	4	C
Vcc	Power Supply Voltage	4.5		5.5	VDC
Err	Data Transmission Error Rate	0		.001	%

Section 6
Physical and User Interface Details

User Interface General Description

The User Interface is the device used by a person to operate the ATC. The User Interface of a controller has traditionally consisted of a keyboard and display, and more recently personal computers and personal digital assistants. For example, the User Interface of a NEMA controller is normally a keyboard and display, with NEMA Port 2 allocated to a personal computer or PDA. A 2070 ATC could use a keyboard and display mounted in the door, or a C60P connector allocated to a personal computer or PDA. Going forward, it is the intent of this specification to:
Preserve compatibility with existing ATC User Interface software
Create a standard for future advanced User Interfaces, such as graphics
Adhere to the ATC API specification for software compatibility

It is not the intent of this specification to:
Preserve User Interface interchangeability among vendors
Dictate User Interface requirements, other than minimum and optional
Limit the choices of User Interfaces

Minimum User Interface

The User Interface performs two separate and necessary functions
User Interface to the Application (Keyboard and Display, for example)
User Interface to the Shell (Updating application software, operating system and API

This document requires a minimum interface to the Application, plus a minimum interface to the Shell. This minimum interface provides a common method to enter data and update software for all hardware and software suppliers. In addition to the specified minimum interface, optional interfaces are allowed. User interfaces not specified here as minimum or optional, are non-compliant.

Minimum User Interface to the Application

The minimum user interface to the Application shall consist of the following:
EIA-232 SP6 connector, 9 pin “D” *(Guidance: C60P of 2070 ATC)*
Data Key

1.1.2 Minimum User Interface to the Shell

The minimum User Interface to the Shell shall consist of the following:
EIA-232 SP4 connector for Shell, 9 pin “D” (*Guidance; C50S of 2070 ATC)*

CPU ACTIVE LED Indicator
Ethernet Port (Guidance: Internal ATC 10/100 hub This should be a switch not a hub Port 2)
USB Port, used only as a memory device

Optional User Interfaces

In addition to the minimum User Interface, the ATC may include one or more optional User Interfaces.

Optional User Interfaces to the Application

Option 1: Keyboard, LCD and Bell *(Guidance: traditional 2070 ATC)*
Option 2: Infrared Port for PDA or Laptop *(Guidance: PDA IRDA COM2)*
Option 3: Ethernet interface to graphics device *(Guidance: Flat panel LCD)*

Optional User Interfaces to the Shell

Option 1: Infrared Port for PDA or Laptop *(Guidance: PDA IRDA COM2)*

Guidance:

SP4 could possibly do "double duty" for both the Application and Shell. For example, the operating system could use SP4 at power up for downloading new application code. The application could also use SP4 as a front panel interface, with the advantage of freeing one serial port for other uses (SP6). However, if this is applied to an Engine Board that is plugged into a 2070 ATC, the front panel data will spew out on C50S instead of controlling the Front Panel. The Application must therefore use the Request Module Status command of the Field I/O determine that the hardware platform is a 2070 ATC requiring the Front Panel data to be redirected to SP6.
Ethernet Port 2 is an uplink for a "straight through" cable to a computer, intended to connect a laptop or PDA for diagnostics or software updates.
Infrared is specified in the "Communications Interfaces" section, compatible with laptop computers and PDAs. Infrared is simply an alternate media to EIA-232, communicating on the same serial port using light instead of cable.
More advanced User Interfaces, such as flat panel LCD or other graphics device may be connected via Ethernet. Hub port 4 is intended for this.
The USB port is to be used for memory devices, only as described in the Engine Board section. Networking is implemented via Ethernet, not via USB.

User Interface Pin Connections

Where are these two shown on the drawing. Can we call them something else or this looks just like another 2070 specification. Lets give them a real name that has some relationship to their purpose/function.

C50S Connector Pinout

Pin	Function
1	C50enabled
2	SP4 RXD
3	SP4 TXD
4	NA
5	DCGND1
6	NA
7	NA
8	NA
9	NA

C60P Connector Pinout

Pin	Function
1	+5VDC
2	SP6 RXD
3	SP6 TXD
4	NA
5	DCGND1
6	NA
7	CPURESET
8	NA
9	CPULED

User Interface Operation

1.4.1 Keyboard, LCD and Bell Operation

1.4.1.1 Keyboard

The Keyboard, at a minimum, shall be capable of the complete single keystroke functionality (without key translations) of the standard ATC 2070 front panel. Each key shall be engraved or embossed with its function character. Key size and spacing shall equal or exceed that of the 2070 ATC, but the actual keypad arrangement is not specified here

1.4.1.2 CPU Active LED Indicator

The cathode of the CPU Active LED Indicator shall be electrically connected to the CPU Activity LED signal and shall have the pull up resistor on the front panel.

1.4.1.3 Display

The Display shall consist of a Liquid Crystal Display (LCD), a backlight and a contrast control. The contrast control can either be a potentiometer or a software controlled contrast adjustment. If using a potentiometer contrast control, the contrast shall increase with clockwise rotation. If using a software controlled contrast, the contrast control shall be accomplished by pressing the (*) key to enable the adjustment, followed by the (+) key to darken and the (-) key to lighten the contrast. By pressing the (*) key again will disable the contrast adjustment. The contrast adjustment shall provide the entire contrast range of the LCD. The Display shall have an LED or EL backlight. The backlight shall be turned on and off by the Controller Circuitry. The backlight and associated circuitry shall consume no power when in off state. The Display shall have at a minimum 8

lines of 40 characters. Each character shall haveminimum dimensions of 2.65 mm wide by 4.24 mm high. Then why do we need this hold over from the 2070? Are the displays on the current NEMA machines this size and shape? Where is our desire to allow for innovation? Why couldn't a vendor use VGA based screen? Why do we have to dictate what this is especially since these units are not interchangeable from manufacturer to manufacturer? The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

1.4.1.4 Cursor

Cursor display shall be turned ON and OFF by command. When ON, the cursor shall be displayed at the current cursor position. When OFF, no cursor shall be displayed. All other cursor functions shall remain in effect.

1.4.1.5 Reset

The User Interface shall be reset once power is applied or have a momentary control reset switch on the PCB that is logic OR'd with the CPU RESET Line, producing a USER Interface RESET. Isn't this determined by the software?

1.4.1.6 Key Press

When a key press is detected, the appropriate key code shall be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code shall be sent. If a key is depressed while another key is depressed, no additional code shall be sent.

1.4.1.7 Auto Repeat

Auto-repeat shall be turned ON and OFF by command. When ON, the key code shall be repeated at a rate of 5 times per second starting when the key has been depressed continuously for 0.5 second, and shall terminate when the key is released or another key is pressed.

1.4.1.8 Special Characters

The controller circuitry shall be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination with the standard ASCII characters. Undefined characters shall be ignored. User-composed characters shall be represented in the communication protocol on Page 9-7-12 in the TEES Put that in this document don't reference TEES anywhere.. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the top pixel in a column and the least significant bit shall represent the bottom pixel. A logic '1' shall turn the pixel ON. There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code

sequence terminated by an "f." If the number of Pn's are more than the number of columns available on the LCD, the extra Pn's shall be ignored. P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.

1.4.1.9 Character Overwrite

Character overwrite mode shall be the only display mode supported. A displayable character received shall always overwrite the current cursor position on the Display. The cursor shall automatically move right one character position on the Display after each character write operation. When the rightmost character on a line position 40) has been overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.

1.4.1.10 Auto Wrap

Auto-wrap shall be turned ON & OFF by command. When ON, a new line operation shall be performed after writing to position 40. When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.

1.4.1.11 Cursor Positioning

Cursor positioning shall be non-destructive. Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.

1.4.1.12 Blinking

Blinking characters shall be supported, and shall be turned ON and OFF by command. When ON, all subsequently received displayable characters shall blink at the rate of 1 Hz with a 60% ON / 40% OFF duty cycle. It shall be possible to display both blinking and non-blinking characters simultaneously.

1.4.1.13 Tab Stops

Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.

1.4.1.14 Auto Scroll

Auto-scroll shall be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one

line. When OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.

1.4.1.15 Displayable Characters

Displayable characters shall be refreshed at least 20 times per second.

1.4.1.16 Backlight Timeout

The Display back light shall illuminate when any key is pressed and shall illuminate or extinguish by command. The backlight shall extinguish when no key is pressed for a specified time. This time shall be program selected by command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals. A value of 1 shall correspond to a timeout interval of 10 seconds. A value of 0 shall indicate no timeout.

1.4.1.17 Command Codes

The Command Codes shall use the following conventions:

Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows:

Pn: Value parameter, to be replaced by a value, using one ASCII character per digit without leading zeros.

P1: Ordered and numbered parameter. One of a listed known parameters with a specified order and number (Continues with P2, P3, etc.)

Px: Display column number (1-40), using one ASCII character per digit without leading zero.

Py: Display line (1-4) one ASCII character ...: Continue the list in the same fashion

Values of 'h' ($68) and 'l' ($6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).

ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.

Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 00 to 7F (7 bits).

1.4.1.18 Communications

The Controller Circuit shall communicate via a SP6 asynchronous serial interface. The interface shall be configured for 38.4 Kbps, 8 data bits, 1 stop bit, and no parity.

1.4.1.19 Bell

The User Interface shall include an electronic bell to signal receipt of ^G (hex 07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.

CONFIGURATION COMMAND CODES

ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py ; Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Home cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn ; Pn…f	1B 50 P1 5B Pn 3B…Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 5 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 5 l	1B 3B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on (Note 2)
ESC [27 l	1B 5B 32 37 6C	Reverse video off (Note 2)
ESC [24 h	1B 5B 32 34 68	Underline on (Note 2)
ESC [24 l	1B 5B 32 34 6C	Underline off (Note 2)
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Clear tab stop Pn = 0,1,2 at cursor = 3 all tab stops
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up

NOTE: 1. Numerical values have one ASCII character per digit without leading zero.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A. Reverse Video is NOT required for Option 3B. Command codes shall be avaliable for option 3C (C60).

INQUIRY COMMAND-RESPONSE CODES

COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Py; Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [B n	1B 5B 42 6E	ESC [P1;P2;.....P6 R	1B 5B P1 3B P2 3B....P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)

1.4.2 EIA-232 Port

The above key codes, configuration command codes and inquiry command-response codes may be conveyed via EIA-232 at the same data rates. In lieu of the keyboard and display, an intelligent device, such as a PDA may be used.

1.4.4 Infrared Port

This option specifies short distance wireless communications via a modulated light beam. Please refer to the IRDA standards for operation.

1.4.5 Ethernet Port

A 10/100 Ethernet port is used for hardwired communications to external devices. Please refer to the IEEE 802.3 standard for operation.

1.4.6 USB Port

USB is used as an interface to memory devices. Refer to USB specification.

1.4.7 Data Key

Datakey Keyceptacle™ (KC4210, KC4210CB or equal) (optional)

User Interface Power Requirements

The User Interface shall be powered by 4.8 to 5.2 VDC. Any additional voltages required by the User Interface, such as backlight and communications, shall be derived from this single power source. The typical and maximum current requirements of each User Interface shall be published for each device.

Power Supply General Description
Could this be optional? Why don't we use the existing cabinet power supply?
The Power Supply shall be an independent module, cooled by convection only. The Power Supply shall be capable of supporting the internal ATC circuitry, plus provide power for each optional module. The Power Supply shall convert 120 VAC at 60 Hz to the proper DC Voltages at the power rating needed to support the unit and any external power as described in Paragraph 2.6.

2.1 "ON/OFF" Power Switch

An "On/Off" POWER Switch shall be provided to disconnect AC from the Power Supply. The "Power On" shall be in the up position.

2.2 LED DC Power Indicators

Four LED DC Power Indicators shall be provided to indicate that all required DC voltages meet the following conditions:
+5 VDC is within +/-5% and the +/- 12 VDC is within +/-8% of their nominal levels.

332 Parallel I/O versions, the +12 VDC isolated shall be within +/-8%.
NEMA versions, the +24 VDC shall be above 21.6 VDC.

2.3 AC Fuse

A replaceable 3AG slow blow fuse shall be provided. Fuse label shall indicate rating.

2.4 +5 VDC Standby Power

+5 VDC Standby Power shall be provided to hold up specified circuitry during the power down period. It shall consist of the monitor circuitry, hold up capacitors, and charging circuitry. A charging circuit shall be provided, that under normal operation, shall fully charge and float the capacitors consistent with the manufacturers' recommendations. The Hold Up power requirements shall be a minimum constant drain of 600 uA at a range of +5 to +2 VDC for over 600 minutes. Capacitors shall be fully charged within 10 minutes.

2.5 Monitor Circuitry

Monitor Circuitry shall be provided to monitor incoming AC Power for Power failure and Restoration and LINESYNC generation.

2.5.1 AC Fail/Power Down

The AC FAIL/POWER DOWN Output Lines shall go LOW (ground true) immediately when the AC service voltage falls below 92 +/-2 VAC. The Lines shall transition to HIGH when the AC service voltage exceeds 97 +/- 2 VAC. The Lines shall be driven separately. The SYSRESET/POWERUP Output Lines shall transition to LOW 525 +/- 25 ms after AC FAIL/POWER DOWN transition to LOW. The Lines shall transition to HIGH 225 +/- 25 ms after Power Restoration and the supply is fully recovered. The Lines shall be driven separately.

2.5.2 Linesync

The 60 Hz Square Wave LINESYNC signal shall be generated by a crystal oscillator, which shall synchronize to the 60-Hz VAC incoming power line at 120 and 300 degrees. A continuous square wave signal shall be +5 VDC amplitude, 8.333 ms half-cycle pulse duration, and 50 +/ - 1% duty cycle. The output shall have drive sink capability of 16 mA. The monitor circuit shall compensate for missing pulses and line noise during normal operation. The LINESYNC shall continue operating after power fail until loss of 5 VDC regulation. LINESYNC crystal oscillator shall have an accuracy of +/- 0.005% at 25 C.

2.6 External Power Supply Requirements

The following external voltages shall be within these parameters.

Each Optional Communications Interface Module:

Voltage	Tolerances	I Minimum	I Maximum
+5 VDC	+4.875 to +5.125 VDC	0.050 AMP	0.500 AMP
+12 VDC	+11.4 to +12.6 VDC	0.050 AMP	0.100 AMP
-12 VDC	-11.4 to –12.6 VDC	0.050 AMP	0.100 AMP

For NEMA TS1 and NEMA TS2 Type 2 versions:

Voltage	Tolerances	I Minimum	I Maximum
+24 VDC	+21.60 to +26.40 VDC	0.050 AMP	0.500 AMP

For 332 Parallel I/O version:

Voltage	Tolerances	I Minimum	I Maximum
+12 VDC ISO	+11.4 to +12.6 VDC	0.050 AMP	0.750 AMP

2.6.1 Line and Load Regulation

The Power Supply shall meet the external voltage tolerances for minimum and maximum loads called out.

332 Parallel I/O Version: 100 VAC to 135 VAC +/- 2 VAC
NEMA: 89 VAC to 135 VAC +/- 2 VAC

2.6.2 Ripple and Noise

Less than 0.5% rms, 2% peak to peak, whichever is greater.

2.6.3 Over Voltage

The Power Supply shall clamp at 130% Vout for all outputs.

2.6.4 Inrush Current

Cold Start Inrush shall be less than 25A at 115VAC.

2.6.5 Holdup Time

The power supply shall supply +5VDC at 0.500 Amps minimum for 550 ms after power loss at 100 VAC. The supply shall be capable of holding up the ATC for two 500 ms Power Loss periods occurring in a 1.5-second period at 100 VAC. Since the Engine Board is powered completely by +5 VDC, no other power supply output voltages need be maintained during power loss to prevent reboot.

Mechanical and Physical General Description

The ATC Mechanical and Physical attributes provide mechanical enclosure and human engineering, including:
Maximum Size
Form Factor
Mounting and Installation Method
Materials
Structural Integrity
Ease of Use
Cost Effectiveness

It is the intent of this specification to:
Preserve compatibility with existing cabinet styles
Reduce the size and complexity of existing controllers
Improve human engineering for intuitive use of complex control functions

It is not the intent of this specification to:
Interchange electronic modules and mechanical assemblies among vendors (except Communications Interface and Engine Board)
Dictate mechanical details
Preserve existing controller sizes and form factors

3.1 Chassis

3.1.1 Construction Materials

The CHASSIS including supports, mounting surfaces, power supply enclosures and front panel shall be made of 0.063-inch minimum aluminum sheet metal or equivalent strength non-corrosive material. Construction materials shall withstand all environmental standards of this specification.

3.1.2 Weight

The total composition weight shall not exceed 25 pounds.

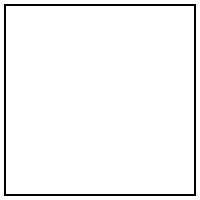
3.1.3 Mounting Method This sounds like one of them stinkin 2070 machines. Why does it have to be rack mounted? What about shelves? Why can't this be a

single card with no enclosure and fit into a detector rack or some other similar sort of arrangement?

As a minimum, the chassis shall be capable of mounting to a Standard EIA 310-B Rack using 4U (or smaller standard increment) open end mounting slots. If not rack mounted, EIA 310-B does not apply and other chassis mounting methods are allowed, not to exceed overall dimensions specified here. Mounting method shall withstand all mechanical shock and vibration requirements of this standard.

Dimensions (All dimensions are given in inches)
No lets not go here!

Details of Maximum Basic Dimensions (not restricted to shape shown)



Note A –

Minimum and Optional components located on front of assembly are as follows:

C50S - 9-Pin DB Socket Type Lets give this a real name representative of its function.
C60P - 9-Pin DB Plug Type Same here!
Infrared Communication Port
Operator Interface (optional)
Keyboard (optional)
ON/OFF Power Switch
Power Supply AC Fuse Holder (with 3AG fuse) Optional!!!!
LED's for each DC power source and "ACTIVE" indications
USB series A 4 Pin Receptacle Communication Port
RJ-45 Connector ETHERNET Port

Note B –

Minimum and Optional components located on rear of assembly are as follows: Here is that stinkin 2070 stuff. Why does this have to be on the rear. Why can't a customer order it with this stuff on the front?

Parallel I/O C1S - M104 Type Can we get rid of these 2070 numbers and give these things a name that means something in plain English?
C11S – 37-Pin Circular Plastic Type

Serial I/O C12S – 25-Pin DB Socket Type
C13S – 25-Pin DB Socket Type

ATC Communications Interface Slots, One or More

Datakey Keyceptacle™ KC4210, KC4210CB or equal (optional)

Eight Ethernet LEDs, two for each of the four switch ports. However, above you state that Ethernet is optional? The one LEDs are labeled "100" and "ACTIVE". Transmitter and Receiver activity is displayed on the "ACTIVITY" LED. The "100" LED is illuminated when the hub port is linked at 100 Mbps and extinguished at all other times. LEDs shall employ clear lenses. Activity light is OK but this 100 light is a complete waste. Nothing else in the Ethernet world does this any longer. Besides what action would you take based upon this indicator. I think nothing. OR whats the "use case" for this indicator?

Section 7
Parallel and Serial I/O Details

1. General Information

The ATC Input / Output (I/O) MAY provide both serial and parallel connections to field devices connected to the ATC, as well as the input of service power. Why should a customer have to have all of these in each machine. These should be modular so that the customer can pick which one is needed for each application. However, if the customer wants to pay for all the connectors he can have them all.

1.1 Parallel Input / Output Overview

The parallel I/O connects the ATC to transportation cabinets including, but not limited to, the following:
NEMA TS-1
NEMA TS-2 Type 1
NEMA TS-2 Type 2
CALTRANS 332
Joint NEMA/AASHTO/ITE/CALTRANS Intelligent Transportation System

Note that this parallel I/O specification does not include Versa Module Europe (VME) or any other parallel high-speed computer bus. Access to devices residing on a high-speed computer bus shall be interfaced via the ATC Ethernet switch port 4 why port 4? It could be any other port the system shouldn't care.. The user is responsible for providing an external rack, power supply, high-speed bus and Ethernet interface module residing in this external rack, as well as all Ethernet software drivers.

1.2 Serial I/O Overview

The serial connections described here provides communications for implementation of existing transportation standards, including but not limited to, the following:
NEMA TS-1
NEMA TS-2 Type 1
NEMA TS-2 Type 2
CALTRANS Type 170
Joint NEMA/AASHTO/ITE/CALTRANS 2070 ATC

1.3 Power Input Overview

The power input provides a service power connection per existing transportation standards, including but not limited to, the following:
NEMA TS-2
NEMA TS-2 Type 1

NEMA TS-2 Type 2
CALTRANS Type 170
Joint NEMA/AASHTO/ITE/CALTRANS 2070 ATC

2. Parallel Input / Output (PI/O)

2.1 Parallel Connection to CALTRANS 332 Style Cabinets

The parallel connection to a CALTRANS 332 Style Cabinet shall consist of the Field Controller Unit, Parallel Input/Output Ports, Connectors C1S, and C11S, and other Module Circuit Functions including muzzle jumper.

2.1.1 Field Controller Unit (FCU)

The FCU shall include a programmable microprocessor/controller unit together with all required clocking and support circuitry. Operational software necessary to meet housekeeping and functional requirements shall be provided resident in socketed firmware or FLASH.

2.1.2 Parallel I/O Ports

The I/O Ports shall provide 64 bits of input using ground-true logic. Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 µA or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to the isolated +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground.

2.1.2.1 Parallel I/O Port Electrical

The I/O Ports shall provide 64 bits of output. Each output written as a logic "1" shall have a voltage at its field connector output of less than 4.0 VDC. Each output written as logic "0" shall provide an open circuit (1 megohm or more) at its field connector output. Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 mA minimum. Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 µs when connected to a load of 100 K-Ohms minimum. Each output circuit shall be protected from transients of 10 ±2 µs duration, ±300 VDC from a 1 K-Ohm source, with a maximum rate of 1 pulse per second.

2.1.2.2 Parallel I/O Port Timing

Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a logic "0" and retain that state until a new writing. The state of all output circuits at the time of Power Up or in Power Down state shall be open. It shall be possible to simultaneously assert all outputs within 100 µs of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

2.1.3 Other Parallel I/O Functions

2.1.3.1 Signals and Capacitive Load

A maximum capacitive load of 100 pF shall be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.

2.1.3.2 Legacy Signal Monitors

An External WDT "Muzzle" Jumper shall be provided internal to the ATC. With the jumper IN and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output Port 5, bit 8 (Connector C1, pin 103 – Monitor Watchdog Timer Input) every 100 ms for 10 seconds or due to CPU Command. When the jumper is missing, the feature shall not apply.

This feature is required to operate with the Model 210 Monitor Unit only. The Model 210 Monitor requires activity on pin 103 immediately after power-up to determine that the ATC is functioning. Without the Muzzle Jumper installed, the ATC boot-up time prevents the application software from performing this task in time. If the controller is truly malfunctioning, the activity on pin 103 ceases within 10 seconds.

More modern Monitors have an adjustable power up time, allowing the intersection to remain in FLASH until the controller has booted-up and the application software begins to toggle pin 103.

2.1.3.3 Watchdog Circuit

A WATCHDOG Circuit shall be provided. It shall be enabled by the software at Power Up with a value of 100 ms. Its enabled state shall be machine readable and reported in the status byte. Once enabled, the watchdog timer shall not be disabled without resetting the PI/O. Failure of the PI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.

2.1.3.4 One KHz Reference

A synchronizable 1 KHz time reference shall be provided. It shall maintain a frequency accuracy of ±0.01% (±0.1 counts per second).

2.1.3.5 Millisecond Counter

A 32-bit Millisecond Counter (MC) shall be provided for "time stamping." Each 1 KHz reference interrupt shall increment the MC.

2.1.3.6 Communications Loss

At Power Up, the FCU loss of communications timer shall indicate loss of communications with the ATC until the user program sends the Request Module Status message to reset the "E" Bit and a subsequent set output command is processed.

2.1.3.7 Control Signals

LINESYNC and POWER DOWN Lines shall be isolated and routed to FCU for shut down functions. CPU RESET and POWER UP (SYSRESET) Lines shall be isolated and logically "OR'd" to form NRESET. NRESET shall be used to reset FCU and other module devices.

2.1.3.8 Isolation

Isolation shall be provided between internal +5DC / DCG#1 and +12 DC ISO/DCG#2. +12 DC ISO shall be used for board power and external logic.

2.1.4 Buffers

A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries. The Transition Buffer shall default to empty. There shall be two entry types: Transition and Rollover. The inputs shall be monitored for state transition. At each transition (If the input has been configured to report transition), a transition entry shall be added to the Transition Buffer. The MC shall be monitored for rollover. At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry shall be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the CPU module upon command. Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer. The entry types are depicted as follows:

Input Transition Entry

Description	msb							lsb	Byte Number
Transition Entry Identifier	S	Input Number							1
Timestamp NLSB	x	x	x	x	x	x	x	x	2
Timestamp LSB	x	x	x	x	x	x	x	x	3

Millisecond Counter Rollover Entry

Description	msb							lsb	Byte Number
Rollover Entry Identifier	1	1	1	1	1	1	1	1	1
Timestamp MSB	x	x	x	x	x	x	x	x	2
Timestamp NMSB	x	x	x	x	x	x	x	x	3

2.1.5 I/O Functions

2.1.5.1 Inputs

2.1.5.1.1 Input Scanning

Input scanning shall begin at I0 (bit 0) and proceed to the highest input, ascending from lsb to msb. Each complete input scan shall finish within 100 µs. Once sampled, the Logic State of input shall be held until the next input scan. Each input shall be sampled 1,000 times per second. The time interval between samples shall be 1 ms ±100 µs. If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer. If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing number. The MC shall be sampled within 10 µs of the completion of the input scan.

2.1.5.1.2 Data Filtering

If configured, the inputs shall be filtered by the FCU to remove signal bounce. The filtered input signals shall then be monitored for changes as noted. The filtering parameters for each input shall consist of Ignore Input Flag and the On and Off filter samples. If the Ignore Input flag is set, no input transitions shall be recorded. The On and Off filter samples shall determine the number of consecutive samples an input must be on and off, respectively, before a change of state is recognized. If the change of state is shorter than the specified value, the change of state shall be ignored. The On and Off filter values shall be in the range of 0 to 255. A filter value of 0, for either or both values, shall result in no filtering for this input. The default values for input signals after reset shall be as follows:

Filtering	Enabled
On and off filter values shall be set to	5
Transition monitoring	Disabled (Timestamps are not logged)

2.1.5.2 Outputs

Simultaneous assertion of all outputs shall occur within 100 µs. Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC. The condition of the outputs shall only be "ON" if the PI/O continues to receive active communications from the CPU Module. If there is no valid communications with the CPU Module for 2.0 seconds, all outputs shall revert to the OFF condition, and the PI/O status byte shall be updated to reflect the loss of communication from the CPU Module.

2.1.5.2.1 Standard Function

Each output shall be controlled by the data and control bits in the CPU Module-PI/O frame protocol as follows:

Output Bit Translation

Case	Output Data Bit	Output Control Bit	Function
A	0	0	Output in the OFF state
B	1	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.
C	0	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF
D	1	0	Output is in the ON state.

2.1.5.2.2 Output Stability

In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured. For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 µs after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle. In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON remain ON until otherwise configured. All outputs shall not glitch nor change state unless configured to do so.

2.1.6 Other Processor Functions

2.1.6.1 Interrupts

All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts. MILLISECOND Interrupt shall be activated by the 1 KHz reference once per ms. A timestamp rollover flag set by MC rollover shall be cleared only on command. LINESYNC Interrupt - This interrupt shall be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal. The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds ($\geq$60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer ($\geq$500 consecutive millisecond interrupts).

2.1.6.2 Communication Service Routine

A low-level communication service routine shall be provided to handle reception, transmission, and communication faults.

2.1.6.3 Communication Processing

The task shall be to process the command messages received from the CPU Module, prepare, and start response transmission. The response message transmission shall begin within 4 ms of the receipt of the received message. Message type processing time constraints shall not exceed 70 ms per message.

2.1.6.4 Input Processing

This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

2.1.7 Data Communications Protocols

2.1.7.1 Protocols

All communication with the CPU Module shall be via command-response protocol. The CPU Module shall always initiate the communication and should the command frame be incomplete or in error, no PI/O response shall be transmitted. The amount of bytes of a command or response is dependent upon the I/O Module identification. The physical interface is not controlled by this specification, and interchangeability among vendors from PI/O to Engine Board is not intended. For example, communications to PI/O module may be implemented via EIA-485 at 614 K bps, 5V TTL, or via a 1 GHz fiber channel, provided all PI/O specifications herein are met, including:
Command and Response Message Content
Command and Response Timing
Error Checking
Electrical Isolation

Therefore, a “frame” is merely a field in the data stream, not related to the physical interface between the CPU and the PI/O.

2.1.7.1.1 Frame Types

The frame type shall be determined by the value of the first byte of the message. The command frames type values $70 - $7F and associated response frame type values $F0 - $FF are allocated to the Contractor diagnostics. All other frame types not called out are reserved. The command-response Frame Type values and message times shall be as follows:

Guidance:

The following Commands and Responses are intended to match the CALTRANS TEES and the Joint NEMA/AASHTO/ITE 2070 ATC commands and responses.

Frame Types

Module Command	I/0 Module Response	Description	Minimum Message Time	Maximum Message Time
49	177	Request Module Status	250 µs	275 us
50	178	MILLISECOND CTR. Mgmt.	222.5 µs	237.5 us
51	179	Configure Inputs	344.5 µs	6.8750 ms
52	180	Poll Raw Input Data	317.5 µs	320 µs
53	181	Poll Filtered Input Data	317.5 µs	320 µs
54	182	Poll Input Transition Buffer	300 µs	10.25 ms
55	183	*Command Outputs*	405 µs	410 µs
56	184	Config. Input Tracking Functions	340 µs	10.25 ms
57	185	Config. Complex Output Functions	340 µs	6.875 ms
58	186	Configure Watchdog	222.5 µs	222.5 µs
59	187	Controller Identification	222.5 µs	222.5 µs
60	188	I/O Module Identification	222.5 µs	222.5 µs
61-62-65 63 64	189-190- 193 191 192	Reserved (note below) Poll variable length raw input Variable length command outputs	 317.5 us 405 us	 320 us 410 us

2.1.7.1.2 ITS Cabinet Frames

Messages 61 / 189, 62 / 190 and 65 / 193 are for ITS Cabinet Monitor Unit. See ITS Cabinet Monitor System Serial Bus #1 for Command and Response Frames. Message 63 / Message 191 shall be the same as Message 52 / 180 except Byte 2 of Message 180 response shall denote the following number of input bytes. Message 64 / 192 shall be the same as Message 55 / 183 except Byte 2 of the Message 55 Command shall denote the number of output data bytes plus the following output data.

2.1.7.2 Request Module Status

The Command shall be used to request PI/O status information response. Command/response frames are as follows:

Request Module Status Command

Description	Msb							lsb	Byte Number
(Type Number = 49)	0	0	1	1	0	0	0	1	Byte 1
Reset Status Bits	P	E	K	R	T	M	L	W	Byte 2

Request Module Status Response

Description	Msb							lsb	Byte Number
(Type Number = 177)	1	0	1	1	0	0	0	1	Byte 1
System Status	P	E	K	R	T	M	L	W	Byte 2
SCC Receive Error Count	Receive Error Count								Byte 3
SCC Transmit Error Count	Transmit Error Count								Byte 4
Timestamp MSB	Timestamp MSB								Byte 5
Timestamp NMSB	Timestamp NMSB								Byte 6
Timestamp NLSB	Timestamp NLSB								Byte 7
Timestamp LSB	Timestamp LSB								Byte 8

2.1.7.2.1 Request Module Status Response

The response status bits are defined as follows:

P - Indicates PI/O hardware reset
E - Indicates a communications loss of greater than 2 seconds
M - Indicates an error with the MC interrupt
L - Indicates an error in the LINESYNC
W - Indicates that the PI/O has been reset by the Watchdog
R - Indicates that the EIA-485 receive error count byte has rolled over
T - Indicates that the EIA-485 transmit error count byte has rolled over
K - Indicates the Datakey has failed or is not present

2.1.7.2.2 Bit Information

Each of these bits shall be individually reset by a '1' in the corresponding bit of any subsequent Request Module Status frame, and the response frame shall report the current status bits. The SCC error count bytes shall not be reset. When a count rolls over (255 - 0), its corresponding roll-over flag shall be set.

2.1.7.3 MC Management Frame

MC management frame shall be used to set the value of the MC. The 'S' bit shall return status '0' on completion or '1' on error. The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

Millisecond Counter Management Command

Description	msb							Lsb	Byte Number
(Type Number = 50)	0	0	1	1	0	0	1	0	Byte 1
New Timestamp MSB	x	x	x	x	x	x	x	x	Byte 2
New Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 3
New Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 4
New Timestamp LSB	x	x	x	x	x	x	x	x	Byte 5

Millisecond Counter Management Response

Description	msb							Lsb	Byte Number
(Type Number = 178)	1	0	1	1	0	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

2.1.7.4 Configure Inputs

The Configure Inputs command frame shall be used to change input configurations. The command-response frames are as follows:

Configure Inputs Command

Description	msb							Lsb	Byte Number
(Type Number = 51)	0	0	1	1	0	0	1	1	Byte 1
Number of Items (n)	n	n	n	n	n	n	n	n	Byte 2
Item # - Byte 1	E	Input Number							Byte 3(I-1)+3
Item # - Byte 2	Leading edge filter (e)								Byte 3(I-1)+4
Item # - Byte 3	Trailing edge filter (r)								Byte 3(I-1)+5

Configure Inputs Response

Description	msb							Lsb	Byte Number
(Type Number = 179)	1	0	1	1	0	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

Block field definitions shall be as follows:

E - Ignore Input Flag. "1" = do not report transitions for this input, "0" = report transitions for this input

e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled)

r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = disabled)

S - return status S = '0' on completion or '1' on error

2.1.7.5 Poll Raw Input Data

The Poll Raw Input Data frame shall be used to poll the PI/O for the current unfiltered status of all inputs. The response frame shall contain 8 or 15 bytes of information indicating the current input status. The frames are as follows:

Poll Raw Input Data Command

Description	msb							lsb	Byte Number
(Type Number = 52)	0	0	1	1	0	1	0	0	Byte 1

Poll Raw Input Data Response

Description	msb							lsb	Byte Number
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

2.1.7.6 Poll Input Filtered Data

The Poll Filtered Input Data frame shall be used to poll the PI/O for the current filtered status of all inputs. The response frame shall contain 8 bytes(-2A) or 15 bytes (2B) of information indicating the current filtered status of the inputs. Raw input data shall be provided in the response for inputs that are not configured for filtering. The frames are as follows:

Poll Filter Input Data Command

Description	Msb							lsb	Byte Number
(Type Number = 53)	0	0	1	1	0	1	0	1	Byte 1

Poll Filter Input Data Response

Description	msb							lsb	Byte Number
(Type Number = 181)	1	0	1	1	0	1	0	1	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

2.1.7.7 Poll Input Transition Buffer

The Poll Input Transition Buffer frame shall poll the PI/O for the contents of the input transition buffer. The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:

Poll Input Transition Buffer Command

Description	msb							lsb	Byte Number
(Type Number = 54)	0	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	X	x	X	x	x	Byte 2

Input Transition Buffer Response

Description	msb							lsb	Byte Number
(Type Number = 182)	1	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	X	x	X	x	x	Byte 2
Number of Entries	x	x	x	X	x	X	x	x	Byte 3
Item #	S	Input Number							Byte 3(I-1)+4
Item # Timestamp NLSB	x	x	x	X	x	X	x	x	Byte 3(I-1)+5
Item # Timestamp LSB	x	x	x	X	x	X	x	x	Byte 3(I-1)+6
Status	0	0	0	0	C	F	E	G	Byte 3(I-1)+7
Timestamp MSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+8
Timestamp NMSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+9
Timestamp NLSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+10
Timestamp LSB	x	x	x	X	x	X	x	X	Byte 3(I-1)+11

2.1.7.7.1 State Transistions

Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. Bit definitions are as follows:

S - Indicates the state of the input after the transition

C - Indicates the 255 entry buffer limit has been exceeded

F - Indicates the 1024 buffer limit has been exceeded

G - Indicates the requested block number is out of monotonic increment sequence

E - Same block number requested, E is set in response

2.1.7.7.2 Block Number

The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module. When the PI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer shall be re-sent to the CPU

Module and the 'E' flag set in the status response frame. If it is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent. If the block number is not incremented by one, the status G bit shall be set. The block number received becomes the current number (even if out of sequence). The Block Number byte sent in the response block shall be the same as that received in the command block. Counter rollover shall be considered as a normal increment.

2.1.7.8 Set Outputs

The Set Outputs frame shall be used to command the PI/O to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to '1'. If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set. Loss of LINESYNC reference shall also be indicated in system status information. The output bytes depend upon field I/O module. These command and response frames are as follows:

Set Outputs Command

Description	Msb							lsb	Byte Number
(Type Number = 55)	0	0	1	1	0	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	X	x	x	X	x	x	x	x	Byte 2
Outputs O8 to O103 Data	X	x	x	X	x	x	x	x	Bytes 3 to 14
Outputs O0 (lsb) to O7 (msb) Control	X	x	x	X	x	x	x	x	Byte 15
Outputs O8 to O103 Control	X	x	x	X	x	x	x	x	Bytes 16 to 27

Set Outputs Response

Description	Msb							lsb	Byte Number
(Type Number = 183)	1	0	1	1	0	1	1	1	Byte 1
Status	0	0	0	0	0	0	L	E	Byte 2

2.1.7.9 Configure Input Tracking Functions

The Configure Input Tracking Functions frame shall be used to configure outputs to respond to transitions on a specified input. Each Output Number identified by Item Number shall respond as configured to the corresponding Input Number identified by the same Item Number. Input to Output mapping shall be one to one. If a command results in more than 8 input tracking outputs being configured, the response V bit shall be set to '1' and the command shall not be implemented. The command and response frames are as follows:

Configure Input Tracking Functions Command

Description	msb							lsb	Byte Number
(Type Number = 56)	0	0	1	1	1	0	0	0	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	E	Output Number							Byte 2(I-1)+3
Item # - Byte 2	I	Input Number							Byte 2(I-1)+4

Configure Input Tracking Functions Response

Description	msb							lsb	Byte Number
(Type Number = 184)	1	0	1	1	1	0	0	0	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp MSB	x	x	x	X	x	x	x	x	Byte 3
Timestamp NMSB	x	x	x	X	x	x	x	x	Byte 4
Timestamp NLSB	x	x	x	X	x	x	x	x	Byte 5
Timestamp LSB	x	x	x	X	x	x	x	x	Byte 6

2.1.7.9.1 Configure Input Tracking Functions Response

Definitions are as follows:

E '1' - Enable input tracking functions for this output
'0' - Disable input tracking functions for this output
I '1' - The output is OFF when input is ON, ON when input OFF
'0' - The output is ON when input is ON, OFF when input is OFF
V '1' - The max. number of 8 configurable outputs has been exceeded
'0' - No error

Number of Items - The number of entries in the frame. If zero, all outputs currently configured for input tracking shall be disabled.

2.1.7.9.2 Timestamp

The timestamp value shall be sampled prior to the response frame.

2.1.7.9.3 Output Updates

Outputs which track inputs shall be updated no less than once per ms. Input to output signal propagation delay shall not exceed 2 ms.

2.1.7.9.4Number of Item Field

The “Number of Item” field is valid from 0 to 16 (most that is sent at one time is 8 enables and 8 disables). If processing a command resulting in more than 8 Input Tracking functions being enabled, none of the command shall be implemented and response message “V” bit set to 1. If an invalid output or input number is specified for a function, the FIOM software shall not do that function definition. It shall also not be counted toward the maximum of 8 input tracking function allowed. The rest of the message shall be processed. When an Input Tracking function is disabled, the output is set according to the most recently received Set Outputs Command. When an input tracking function for an output is superseded (redefined as either another input tracking

function, or as a complex output function) nothing shall be done with the output. The most recent value remains until the new function changes it.

2.1.7.10 Configure Complex Output Functions

The Configure Complex Output Functions frame shall be used to specify a complex output for one to eight of any of the outputs. If a Configure Complex Output Function command results in more than eight outputs being configured, the 'V' bit in the response message shall be set to a '1', and the command shall not be implemented. Two output forms shall be provided, single pulse and continuous oscillation. These output forms shall be configurable to begin immediately or on a specified input trigger and, in the case of continuous oscillation, to continue until otherwise configured or to oscillate only while gated active by a specified input. If the command gate bit is active, the command trigger bit shall be ignored and the specified input shall be used as a gate signal. The command and response frames are as follows:

Configure Complex Output Functions Command

Description	msb							lsb	Byte Number
(Type Number = 57)	0	0	1	1	1	0	0	1	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	0	Output Number							Byte 7(I-1)+3
Item # - Byte 2	Primary Duration (MSB)								Byte 7(I-1)+4
Item # - Byte 3	Primary Duration (LSB)								Byte 7(I-1)+5
Item # - Byte 4	Secondary Duration (MSB)								Byte 7(I-1)+6
Item # - Byte 5	Secondary Duration (LSB)								Byte 7(I-1)+7
Item # - Byte 6	0	Input Number							Byte 7(I-1)+8
Item # - Byte 7	P	W	G	E	J	F	R	L	Byte 7(I-1)+9

Configure Complex Output Functions Response

Description	msb							lsb	Byte Number
(Type Number = 185)	1	0	1	1	1	0	0	1	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp (MSB)	x	x	x	x	x	x	x	x	Byte 3
Timestamp (NMSB)	x	x	x	x	x	x	x	x	Byte 4
Timestamp (NLSB)	x	X	x	x	x	x	x	x	Byte 5
Timestamp (LSB)	x	X	x	x	x	x	x	x	Byte 6

2.1.7.10.1 Configure Complex Outputs Bit Fields

The bit fields of the command frame are defined as follows:

E '1' - enable complex output function for this output

'0' - disable complex output function for this output

J '1' - During the primary duration, the output shall be written as a logic '1'. During the secondary duration, the output shall be written as a logic '0'.

'0' - During the primary duration, the output shall be written as a logic '0'. During the secondary duration, the output shall be written as a logic '1'.

Output Number - 7-bit output number identifying outputs

Primary Duration - For single pulse operation, this shall determine the number of 'ticks' preceding the pulse. For continuous oscillation, this shall determine the length of the inactive (first) portion of the cycle.

Secondary Duration - For single pulse operation, this shall determine the number of 'ticks' the pulse is active. Subsequent to the secondary duration, the output shall return to the state set according to the most recently received Set Outputs command. For continuous oscillation, this shall determine the length of the active (second) portion of the cycle. 0 = hold output state until otherwise configured.

F '1' - The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.

'0' - The trigger or gate shall be derived from the raw input.

R '1' - For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.

'0' - For triggered output, the output shall be triggered by an OFF-to-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON.

Input Number - 7-bit input number identifying inputs 0 Up.

P '1' - The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.

'0' - The output is configured for continuous oscillation.

W '1' - It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.

'0' - Operation shall begin within 2 ms of the command receipt.

G '1' - Operation shall be gated active by the specified input.

'0' - Gating is inactive.

L '1' - The LINESYNC based clock shall be used for the time ticks.

'0' - The MC shall be used for the time ticks.

V '1' - Indicates maximum number of configurable outputs is exceeded.

'0' - No error

Number of items - The number of entries in the frame. If 0, all outputs currently configured as complex outputs shall be disabled.

2.1.7.10.2 Sampling Rate

Controlling input signals shall be sampled at least once per millisecond.

2.1.7.10.3 Data Range

The "Number of Items" field is valid from 0 to 16. Zero means disable all Complex Output functions. Sixteen is the maximum because the most that is sent at one time is 8 enables and 8 disables. If processing a command results in more than 8 Complex Output functions being enabled, none of the command shall be implemented and the response message "V" bit shall be set to 1. If an invalid output or input number (the "G" or "W" bits being set to 1) is specified for a function, that function definition is not done by the FIOM software. It shall also not be counted towards the maximum of 8 Complex Output functions allowed. The rest of the message shall be processed. When a Complex Output function is disabled, the output is set according to the most recently received Set Outputs command. When a complex output function for an output is superseded, that is, redefined as wither another Complex Output function, or as an Input Tracking function, nothing special is done with the output. The most recent value remains until the new function changes it. The "G" bit (gating) set to 1 takes precedenceover the "W" bit (triggering). If gating is ON, triggering is turned OFF, regardless of the value of the "W" bit in the command message. If a Complex Output is configured with the "G" bit set to 1 (gating) and the "P" bit set to 0 (continuous oscillation), the output is set to OFF (0) whenever the specified input changes state so that the oscilla tion should cease (output inactive). For a single pulse operation ("G" bit set to 1), after the secondary duration completes the Complex Output function shall be disabled, and the output shall be set according to the most recently received Set Outputs command.

2.1.7.11 Configure Watchdog

The Configure Watchdog frames shall be used to change the software watchdog timeout value. The Command and response frames are as follows:

Configure Watchdog Command

Description	msb							lsb	Byte Number
(Type Number = 58)	0	0	1	1	1	0	1	0	Byte 1
Timeout Value	x	x	x	x	x	x	x	x	Byte 2

Configure Watchdog Response

Description	msb							lsb	Byte Number
(Type Number = 186)	1	0	1	1	1	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	Y	Byte 2

2.1.7.11.1 Timeout Value

The timeout value shall be in the range between 10 to 100 ms. If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.

2.1.7.11.2 Time Out Change

On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the "Y" bit set. The response frame bit (Y) shall indicate a '1' if the watchdog has been previously set and a '0' if not.

Controller Identification

This is a legacy message command / response for PI/O modules with Datakey resident. Upon command, a response frame containing the 128 bytes of the Datakey. On NRESET transition to High or immediately prior to any interrogation of the Datakey, the PI/O shall test the presence of the Key. If absent, the PI/O Status Bit "K" shall be set and no interrogation shall take place. If a error occurs during the interrogation, Bit "K" shall be set. If "K" bit set, only the first two bytes shall be returned. The Command Response frames are as follows:

Controller Identification Command

Description	msb							lsb	Byte Number
Type Number= 59	0	0	1	1	1	0	1	1	Byte 1

Controller Identication Response

Description	msb							lsb	Byte Number
Type Number = 187	1	0	1	1	1	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	K	Byte 2
Datakey	x	x	x	x	x	x	x	x	Bytes 3 to 130

Module Identification

The PI/O Identification command frame shall be used to request the PI/O Identification value Response of "1" for the 332 PI/O, "2" for the TS-2 Type2 PI/O, 3 for the TS-2 Type 1 PI/O. The Identification value response for ITS Cabinet SIUs and CMU shall be frame address. The command and response frames are shown as follows:

I/O Module Identification Command

Description	msb							lsb	Byte Number
(Type Number = 60)	0	0	1	1	1	1	0	0	Byte 1

I/O Module Identification Response

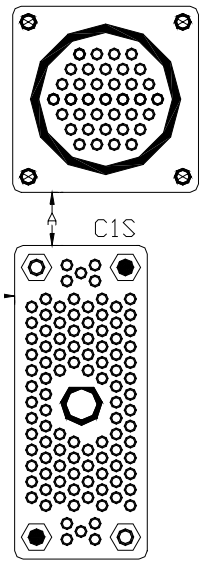
Description	msb							lsb	Byte Number
(Type Number = 188)	1	0	1	1	1	1	0	0	Byte 1
PI/O I D byte	x	x	x	x	x	x	x	x	Byte 2

2.1.7 Mechanical Details

C11S

NOTES:

1. C1S Dark Circles denote guide pin locations



C1S and C11S Pin Configuration: Refer to CALTRANS TEES

2.2 Parallel Connection to NEMA TS-1 or TS-2 Type 2 Cabinets

2.2.1 Description

This PI/O shall consist of an FCU Controller, Parallel Input / Output Ports, Field Connectors and Communications Circuits. It is similar in function to the 332 style PI/O, except it provides more inputs and outputs via different physical connectors.

2.2.2 Front Panel

The Front Panel shall be furnished with the following:

Incoming VAC fuse protection
Four NEMA Connectors, A, B, C & D

2.2.3 Functional Requirements Exceptions

This PI/O shall meet all requirements under Paragraph 2.1, including all subparagraphs, with the following exceptions:
118 bits of input and 102 bits of output shall be provided.
Specification for inputs applies, except the voltage is +24 V in lieu of +12 V
Ground False, “0”, exceeds 16.0 VDC.

Fault Monitor and Voltage Monitor

NEMA TS-2 Controller FAULT and VOLTAGE Monitor functions (outputs to the cabinet monitor) shall be provided.

Monitor Logic

Two 3-input OR gates shall be provided. The gate 1 output shall be connected to Connector A, Pin A (FAULT MONITOR) and gate 2 output shall be connected to Connector A, Pin C. Any FALSE state input shall cause a gate output FALSE (+24 V) state.

2.2.4.2 Watchdog

The FCU Port 10, Bit 7 output shall normally change its state every 100 mS. A Watchdog Timer (WDT) circuit shall monitor the output. No state change for 2 +/- 0.1 second shall cause the circuit output to generate a FALSE (+24 VDC) output (input to gates 1 and 2). Should the FCU begin changing state, the WDT output shall return to TRUE (0 VDC) state.

2.2.4.3 The 5 VDC Monitor

5 VDC shall be monitored. When 5 VDC supply falls out of regulation (+/- 0.25 V), this monitor circuit shall generate a FALSE output (input to gates 1 and 2) Normal operation shall return the output state to TRUE state.

Fault Monitor Logic

The FCU microprocessor output shall be assigned to FAULT Monitor (input to gate 1) and another output shall be assigned to VOLTAGE MONITOR (input to gate 2).

Monitor Control from Application Software

CPU Port 5 SET OUTPUT COMMAND Message OUTPUTs O78 and O79 shall be assigned to FAULT (O78) and VOLTAGE (O79). The bit logic "1" shall be FCU output FALSE.

Monitor Output Power Up Conditions

CPU / FCU operation at POWER UP shall be as follows:

FCU Comm Loss Flag set. FAULT & VOLTAGE MONITOR outputs set FALSE.
CPU REQUEST MODULE STATUS COMMAND Message with "E" bit set is sent to FCU to clear Comm Loss Flag and responds to CPU with "E" bit reset.
Before the Comm Loss timer expires, the SET OUTPUTS COMMAND data must be sent. In that data, the O78 and O79 logically set to "0" will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted a the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.
If the above message sequence is not followed, Comm Loss Flag shall be set (or remain) and VM & FM shall retain the FALSE output state.
Performs items 2 & 3 above User Software.

Communications Loss

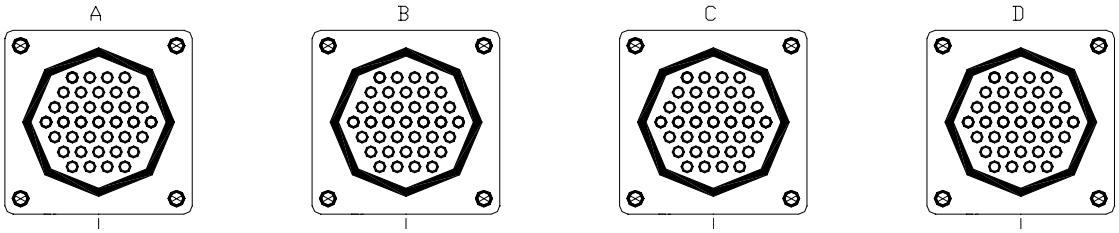
A CPU/FCU Communications Loss during normal operation shall cause all outputs to go blank (FALSE state) and shall set the Comm Loss Flag. FM and VM outputs shall be in the FALSE state.

Mechanical Details

Connector A, B, C Pin Configurations: Refer to NEMA TS-2 Specification

Connector D Pin Configuration: Refer to CALTRANS TEES

Connector Diagram:



NOTES:

1. **A = NEMA "A" Connector, Type MS-3112-22-55P**
2. **B = NEMA "B" Connector, Type MS-3112-22-55S**
3. **C = NEMA "C" Connector, Type MS-3112-24-61S**
4. **D = NEMA "D" Connector, Type MS-3112-24-61P**
5. **Spacing Between A, B, C, D Connectors = 3.0 " min, Center to Center.**

2.3 Parallel Connection to NEMA TS-2 Type 1 Cabinets

2.3.1 Description

The TS-2 Type 1 PI/O provides a TS2-1 compatible interface, AC Power to the ATC, Fault Monitor Logic Output and Output Frame Byte 9 Bit 6 to the NEMA TS2 Cabinet Monitor Unit (CMU).

2.3.2 Front Panel

The Front Panel shall be furnished with the following:

Incoming VAC fuse protection
One NEMA Connector, A
One AC Outlet for ATC Line Cord

2.3.3 Functional Requirements Exceptions

This PI/O shall meet all requirements under Paragraph 2.1, including all subparagraphs, with the following exceptions:

No C1 and C11 Connectors on the front panel of the module

No 64 inputs / 64 outputs requirements

2.3.4 Parallel Connector

The parallel connector is a 10 Pin NEMA Connector A

2.3.5 Service Power Connection

Incoming 2070 AC Power is derived from Connector A Pin C (AC+), Pin A (AC-), and Pin H (Equipment Ground). The power is directly routed to the NEMA 5-15 Receptacle. Connector A shall intermate with a NEMA TS2 Type 1 (MS3106O-18-1S) cable.

2.3.6 Fault Monitor

An FCU output shall drive a open collector transistor whose output shall be routed to Connector A Pin F for use as a FAULT MONITOR Output. The transistor shall be capable of sinking 200 ma at 30 VDC.

2.3.7 Connector A Pin Assignment

Connectors A pin assignment: Refer to NEMA TS-2 Specification

3. Serial Input / Output (SI/O)

The ATC provides as minimum of 10 serial ports as follows:

Four synchronous or asynchronous ports designated SP1, SP2, SP3 and SP8
Two asynchronous ports, designated SP4 and SP6
One Ethernet port operating at a minimum rate of 10 Mbps, designated Ethernet
One synchronous port designated SP5
One Serial Peripheral Interface (SPI) compatible port designated SP9.
One Universal Serial Bus (USB) port designated SP10.

Guidance: The traditional use of the serial ports is as follows:

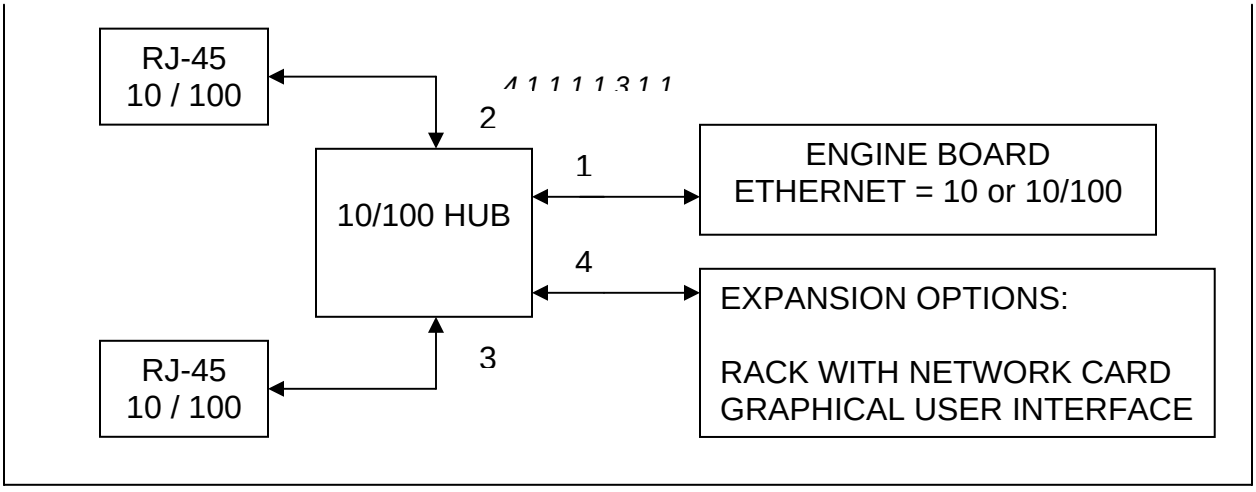
SP1: External communications, via slot A2, top connector
SP2: External communications, via slot A2, bottom connector
SP3: ITS Cabinet SB2, via C21S, or external communication via slot A1 top connector
SP4: OS console via C50S or slot A1 bottom connector
SP5: Field I/O communications module
SP6: User Interface, or via C60P
SP8: Field I/O communications via C13S connector
SP9: Portable Memory Device (Data Key)
SP10: Peripheral USB devices

Refer to Engine Board section for a description of each serial port operation.

How does this follow the above stuff?
Engine Board Ethernet shall support communications at a rate of 10 Mbps minimum. The Engine Board shall contain all Ethernet circuitry including PHY and transformer (refer to Engine Board section). Each ATC shall be "Ethernet Ready" with IP Who will assign this address? What if my system implements DHCP and this address constantly changes? and MAC addresses Whose OUI will be in this address the Engine board makers or the controller makers? Whose will be in each port on the Ethernet Switch?. The supplied local area network communications software shall provide a small footprint Internet protocol stack that enables the ATC to communicate with other computer systems connected to a TCP/IP network. This enables application software to send data, receive data, and log on to other computer systems. The ATC shall support the User Datagram Protocol (UDP), Transmission Control Protocol (TCP), Internet Protocol (IP), as well as a raw socket interface. Standard TCP/IP client/server applications such as inetd, telnet(d) and ftp(d) are provided with this software along with network administration tools such as ifconfig, netstat and ping. The ATC Ethernet does not by default define actual Internet data transmission protocols. These must be configured for each networking environment. Refer to application software specifications for installation and operation.

ATC shall provide an internal 4-port 10/100 switch. Ports shall be allocated as follows: Why do you feel the need to assign ports? Why not let the higher level protocols decide what is plugged into to each port. This type of thing will complicate the software and cause potential troubleshooting nightmares.
Port 1: Internal Downlink Port to Engine Board, either 10 or 10/100 BPS
Port 2: Front Panel RJ-45 Uplink Port to Laptop, 10/100 BPS
Port 3: Front Panel Downlink Port to Communications Backbone (ie NTCIP)
Port 4: Downlink Port to Optional Expansion Rack NIC (ie VME)

Pictorially:



If you use a hub the only packets that the cpu will not see coming from the hub are the ones it sends there. A hub sends each packet to all hub ports except the one that the

packet is being received from. A hub acts exactly like the coaxial cable that it replaced. If one of the hub ports is used to forward packedtized video images the cpu will most certainly be flooded with them just like every other port on the hub. This could have a huge negative impact on the cpu.

4 Power Inputs

4.1 NEMA Power Inputs

Service power inputs for NEMA ATC versions may be via the NEMA "A" connector. Does it have to? Why can't I have a machine with a separate power cord for NEMA applications? To me this would hamper the flexibility of the machine. Also why couldn't I use an existing low voltage power supply elsewhere in the cabinet?

4.2 Power Inputs, Other ATC Configurations

Service power inputs for all versions other than NEMA may be via a three #16 conductor power cable, 3 ft minimum length, and permanently attached to the ATC with a strain relief. The end plug connector shall be a three blade NEMA 5-15P grounding plug.

Section 8
ATC 3000 Test Procedures
(to be added later)

Section 9
Cross-Reference of ATC 3000 Functional Requirements
(to be supplied 3/21/2003)

Section 10
Definitions

A - Ampere

AC - Alternating Current

AC+ - 120 Volts AC, 60 hertz ungrounded power source

AC- - 120 Volts AC, 60 hertz grounded return to the power source

ANSI - American National Standard Institute

ASCII - American Standard Code for Information Interchange

Assembly - A complete machine, structure or unit of a machine that was manufactured by fitting together parts and/or modules

ASTM - American Society for Testing and Materials

AWG - American Wire Gage

C - Celsius

C Language - The ANSI C Programming Language

Cabinet - An outdoor enclosure generally housing the controller unit and associated equipment

Certificate of Compliance - A certificate signed by the manufacturer of the material or the manufacturer of assembled materials stating that the materials involved comply in all respects with the requirements of the specifications

Channel - An information path from a discrete input to a discrete output

CMOS - Complementary Metal Oxide Semiconductor

Component - Any electrical or electronic device

Controller Unit - That portion of the controller assembly devoted to the operational control of the logic decisions programmed into the assembly

CPU - Central Processing Unit

CRC - Cyclic Redundancy Check

dB - Decibel

dBa - Decibels above reference noise, adjusted

DC - Direct Current

DIN - Deutsche Industrie Norm

DMA - Direct Memory Access

EG - Equipment Ground

EIA - Electronic Industries Association

EMI - Electro Magnetic Interference

EPROM - Ultraviolet Erasable, Programmable, Read Only Memory Device

EEPROM - Electrically Erasable, Programmable, Read Only Memory Device

Equal - Connectors: comply to physical dimensions, contact material, plating and method of connection.
Devices: conforming to function, pin out, electrical and operating parameter requirements, access times and interface parameters of the specified device

ETL - Electrical Testing Laboratories, Inc.

Firmware - A computer program or software stored permanently in PROM, EPROM, ROM or semi-permanently in EEPROM

FLASH - A +5 VDC powered IC Memory Device with nonvolatile, electrically erasable, programmable, 100K read/write minimum cycles and fast access time features

FPA - Front Panel Assembly

HEX	-	Hexadecimal
Hz	-	Hertz
IC	-	Integrated Circuit
I.D.	-	Identification
IEEE	-	Institute of Electrical and Electronics Engineers
ISO	-	International Standards Organization
Jumper	-	A means of connecting/disconnecting two or more conductive by soldering/desoldering a conductive wire or by PCB post jumper
KB	-	Kilobytes
LED	-	Light Emitting Diode
LOGIC	-	Negative Logic Convention (Ground True) State
LSB	-	Least Significant Byte
lsb	-	Least Significant Bit
MB	-	MegaByte
MSB	-	Most Significant Byte
msb	-	Most Significant Bit
m	-	Milli (one one thousandth)
MCU/MPU/ IMP	-	Micro Controller Unit, Microprocessor Unit, or Integrated Multiprotocol Processor
MIL	-	Military Specifications
MODEM	-	Modulation/Demodulation Unit
Module	-	A functional unit that plugs into an assembly
Motherboard	-	A printed circuit connector interface board with no active or

passive components

MOS - Metal-Oxide Semiconductor

MOV - Metal-Oxide Varistor

MS - Military Standards

N - Newton: SI unit of force

NA - Presently Not Assigned. Cannot be used by the contractor for other purposes

NEMA - National Electrical Manufacturer's Association

n - nano (one million one thousandths)

NLSB - Next Least Significant Byte

nlsb - Next Least Significant Bit

NMSB - Next Most Significant Byte

nmsb - Next Most Significant Bit

PCB - Printed Circuit Board

PLA/PAL - Programmable Array Logic Device

Power Failure - A Power Failure is said to have occurred when the incoming line voltage falls below 92 +/- 2 VAC for 50 ms. See Power Conditions.

Power Restoration - Power is said to be restored when the incoming line voltage equals or exceeds 97 +/- 2 VAC for 50 ms. See Power Conditions.

Power Conditions - 16.7 ms (one 60 Hz cycle) reaction period is allowed to be included in the 50 ms timing or added to (67 ms duration). The hysteresis between power failure and power restoration voltage settings shall be a min. of 5 VAC with a threshold drift of no more than 0.2 VAC.

ppm - Parts per million

PWM - Pulse Width Modulation

RAM - Random Access Memory

RDR	-	ACIA Receiver Data Register
RF	-	Radio Frequency
RMS	-	Root-Mean-Square
ROM	-	Read Only Memory Device
RTS	-	Request to Send
SCC	-	Serial Communications Controller
SCI	-	Serial Communications Interface
SDLC	-	Synchronous Data Link Control
S	-	Logic State
s	-	second
Second Sourced	-	Produced by more than one manufacturer
SRAM	-	Static Random Access Memory Device
SW	-	Switch
TOD	-	Time Of Day Clock
TTL	-	Transistor-Transistor Logic
µ	-	Micro
UL	-	Underwriter's Laboratories, Inc.
VAC	-	Voltage Alternating Current
VDC	-	Voltage Direct Current
VME	-	Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2
x	-	Number Value
XX	-	Manufacturer's Option

WDT - Watchdog Timer: A monitoring circuit, external to the device watched, which senses an Output Line from the device and reacts